Non-isolated & regulated 40A single output POL Digital Regulators

PMBus Patent Protection RoHS

3 years Warranty

- ASICs, FPGA, ARM
- Network processor
- AI processor
- Distributed power supply
- Communication equipment
- Servers and storage devices

FEATURES

- Wide input voltage range: 4.5-14.4VDC, including 5V, 12V universal input
- Wide output voltage range: 0.6 to 4.5VDC, digital adjustment can be reduced to 0.48V
- 40A output current
- Support parallel connection up to 80A
- High output voltage deviation 2mV
- Output ripple as low as 4 mVp-p, 1.2Vout, 100%Io
- PMBus digital communication protocol
- Operating temperature range: -40 ℃ to +85 ℃
- Efficiency up to 95%, 7.5Vin, 3.3Vout, 100%Io, loss only 5.9W
- Remote control, PGOOD, remote compensation, clock synchronization functions
- Input under-voltage, output over/under-voltage protection functions
- Output over-current, short circuit, over-temperature protection functions
- Configure and monitor using PMBus

The KD12T-40A digital modules are non-isolated 40A single output POL power supply, it can work in a wide input voltage range of 4.5-14.4VDC, compatible with front-end 5V/12V input system. It provides an output of precisely adjustable 0.45-4.5VDC voltage through external analog voltage divider, it features PMBus digital control, in addition, it also has PMBus® communication protocol, remote control, PGOOD, remote compensation, clock synchronization, multi-module parallel functions, and with input over/under-voltage, output over/under-voltage, output over-current, short circuit, over-temperature and other protections, the host computer can realize human-computer interaction, it provides a large number of operating instructions to control and monitor the module, and it has the characteristics of high voltage accuracy, low output ripple, and high dynamic response.

Note: ①Use the host computer together, please refer to website for details, and contact FAE for technical support consultation.

Selection Guide

Certification	Part No.	Input Voltage (VDC)	Output Voltage① (VDC)	Output Current (A) Max.	Output Voltage Accuracy (mV)	Efficiency (Nominal, Full Load, Typ.)	Ripple (Vo=1.2)
		Nominal (Range)			Nominal		Nominal, Full Load
--	KD12T-40A	12 (4.5-14.4)	(0.6-2.0)	40	±2	91.5% (Vo=1.8)	4mVp-p
		12 (7.5-14.4)	(2.0-3.3)	34	±2	94.0% (Vo=3.3)	
			(3.3-4.5)	20	±2	92.5% (Vo=4.5)	

Note:
① The default output of module is 0.6V. For threshold fine-tuning, see PMBus operation Guide. For simulation adjustment, see TRIM adjustment function.

Limit Rating

Parameter		Min.	Max.	Unit
Voltage	VIN	-0.3	15	V
	NC, TRIM, PG, ON/OFF, SHARE3, SHARE1	-0.3	7	
	VS-, VS+, DATA, SMBALERT#, CLK, SYNC, SHARE, SHARE2	-0.3	5.5	
	ADDRESS 0, ADDRESS 1	-0.3	3.6	

Note:
1. Exceeding the stress values listed in the "Maximum Rating" table may cause permanent damage to the device. The reliability of the device may be affected under the limit rated conditions for a long time. All voltage values are based on GND.
2. The power module can be used in a variety of applications, from simple independent power supply to complex distributed power supply architecture. In order to maintain the maximum flexibility, the internal fuse is not included, but in order to achieve the maximum security and system protection of the system, it is recommended to add a fuse at the input end (maximum rating is recommended to be 35A).

Eectrical Characteristics

Item	Operating Conditions		Min.	Typ.	Max.	Unit
Input Voltage Range			4.5	12	14.4	VDC
Output Voltage Range	Through the external resistance divider		0.6	--	4.5	
PMBus Output Voltage Range	Digital adjustment		0.48	--	4.5	
Input Current Max.	100% load		--	--	20	A
Output Current Max.			--	--	40	
Output Over-current Protection Threshold (The PMBus Can Be Used For Adjustment)	0.6-3.3		--	58	--	
	3.3-4.5		--	35	--	
Input Current No-load (Module Enabled)	Nominal Voltage input, 0% load, Vo=0.6V		--	78	--	mA
	Nominal Voltage input, 0% load, Vo=3.3V		--	220	--	
ON/OFF The input current is turned off			--	12	--	
Output Voltage Deviation	0.6-2.0VDC		--	2	--	mV
	2.0-4.5VDC		--	5	--	
Linear Adjustment Deviation	Vo=0.6VDC		--	1	--	
	Vo=1.2VDC		--	1	--	
	Vo=1.8VDC		--	1	--	
	Vo=3.3VDC		--	1	--	
	Vo=4.5VDC		--	1	--	
Load Adjustment Deviation	Vo=0.6VDC		--	1	--	
	Vo=1.2VDC		--	1	--	
	Vo=1.8VDC		--	2	--	
	Vo=3.3VDC		--	2	--	
	Vo=4.5VDC		--	2	--	
Output Voltage Ripple & Noise	20Mhz, measurement method	0.6VDC	--	4	--	mVp-p
		1.2VDC	--	10	--	
		1.8VDC	--	18	--	
		3.3VDC	--	25	--	
		4.5VDC	--	30	--	
Dynamic Load	20Mhz, measurement method	0.6VDC, 100A/us, 10A-30A-10A	--	±18	--	mV
		1.2VDC, 100A/us, 10A-30A-10A	--	±36	--	
		1.8VDC, 100A/us, 10A-30A-10A	--	±54	--	
		3.3VDC, 100A/us, 8.5A-25.5A-8.5A	--	±99	--	
		4.5VDC, 100A/us, 5A-15A-5A	--	±135	--	
Temperature Coefficient			--	±0.4	--	%/℃
Capacitive Load(μF) Max.			--	--	10000	μF

Efficiency	Vin=12VDC, 50% load	Vo=0.6VDC	--	81.0	--	%
		Vo=1.2VDC	--	89.5	--	
	Vin=12VDC, 50% load	Vo=1.8VDC	--	91.5	--	
		Vo=3.3VDC	--	93.5	--	
		Vo=4.5VDC	--	92.5	--	
	Vin=5VDC, 50% load	Vo=0.6VDC	--	87.1	--	
		Vo=1.2VDC	--	90.4	--	
		Vo=1.8VDC	--	93.0	--	
	Vin=7.5VDC, 50% load	Vo=3.3VDC	--	95.2	--	
		Vo=4.5VDC	--	94.0	--	
	Vin=12VDC, 100% load	Vo=0.6VDC	78.0%	82.5	--	
		Vo=1.2VDC	84.0%	88.5	--	
		Vo=1.8VDC	86.5%	91.5	--	
		Vo=3.3VDC	89.0%	94.0	--	
		Vo=4.5VDC	87.5%	92.5	--	
	Vin=5VDC, 100% load	Vo=0.6VDC	--	82.5	--	
		Vo=1.2VDC	--	88.5	--	
		Vo=1.8VDC	--	91.5	--	
	Vin=7.5VDC, 100% load	Vo=3.3VDC	--	95.0	--	
		Vo=4.5VDC	--	94.0	--	
Loss	Vin=12VDC, 100% load	Vo=0.6VDC	--	5.0	--	W
		Vo=1.2VDC	--	6.2	--	
		Vo=1.8VDC	--	7.1	--	
		Vo=3.3VDC	--	7.4	--	
		Vo=4.5VDC	--	8.3	--	
Module Frequency			--	560	--	kHz
SYNC	Switching frequency (default value)		500	--	1500	
	Switching frequency range		2.0	--	--	V
	SYNC high-level threshold		--	--	0.8	
	SYNC low-level threshold		100	--	--	ns
	Minimum SYNC pulse width		--	--	10	
Remote Control Positive Logic ON/OFF	Pulled high(Module on)		3.5	--	5	V
	Pulled low(Module off)		0	--	0.5	
	Turn off current		--	--	1	μA
Remote Control Negative Logic ON/OFF	Pulled high(Module off)		3.5	--	5	V
	Pulled low(Module on)		0	--	0.5	
	Turn off current		--	--	1	μA
Input Under-voltage Protection	Open threshold		--	4.25	--	V
	Turn Off Threshold		--	4.0	--	
	PMBus Instruction adjustable range		4..25	--	14	
Output Over-voltage Protection	TRIM Threshold		--	800	--	mV
Output Under-voltage Protection	TRIM Threshold		--	528	--	
Output Over-temperature Protection			--	130	--	%

Note:
1. This module adopts digital control, which includes a configuration file, which affects the function and performance of the module. Unless otherwise stated, all specifications are in the default configuration file. If the configuration file needs to be changed, please refer to the following PMBus instruction information. The positive and negative logic of the module in the above table can be modified through digital control;
2. Unless otherwise stated, the above specifications are determined by peripheral Cin = 2x680μF/10mΩ//10x10μF, Co=1x0.1μF//5x47μF/2x22μF//680μF//4x100μF;
3. Unless otherwise stated, the output voltage is tested on the output pin of the product;
4. Unless otherwise stated, the above specifications apply to 1.2V output;
5. Changing switching frequency will affect module performance. Please confirm with FAE before changing;
6. The external synchronous clock pin signal must be a square waveform with a duty cycle of 50%.

PMBus Digital Characteristics

Item	Operating Conditions	Min.	Typ.	Max.	Unit
Upper Computer Signal Characteristics					
Over-temperature Protection		--	130	--	℃
PMBus Temperature Control Range		120	--	160	
Input Under-voltage Protection PMBus Adjustable Range		4.25	--	14	V
Output Voltage Adjustable Step		--	2	--	mV
TRIM Adjustable Threshold Range		500	600	800	mV
PGOOD Characteristics					
PGOOD Threshold Accuracy		-4	--	4	%
Upper Computer Measurement Characteristics					
Upper Computer Output Voltage Measurement Range		0.48	--	4.5	V
Upper Computer Output Voltage Offset Voltage		--	0.1	--	
PC Output Voltage Measurement Accuracy	Vo=1V	-0.8	--	0.8	%
Upper Computer Output Current Measurement Range		0	--	40	A
Output Current Measurement Deviation of Upper Computer	Io≥20A, IOUT_CAL_GAIN=0.503mΩ	-640	--	640	mA
Note: The above contents are related specifications of PMBus digital configuration. For details, see Application recommendation.					

INITIALIZATION TIME AND SOFT-START						
t_{ss}	Soft-start time(1)	Default settings	--	2.7	--	ms
	Programmable range		0.6	--	9	ms
(1) The soft-start time is the time that the internal reference voltage rises from 0 V to 600 mV.						
UVLO						
$V_{IN(on)}$	Input turn-on voltage	Default settings	--	4. 25	--	V
$V_{IN(off)}$	Input turn-off voltage	Default settings	--	4	--	V
$V_{INON(rng)}$	Programmable range for turn on voltage		4.25	--	14	V
$V_{INOFF(rng)}$	Programmable range for turn off voltage		4	--	13.75	V
Note: Hysteresis of at least 150 mV is specified by design.						
OUTPUT over-voltage / under-voltage						
V_{FBOV}	Trim pin over voltage threshold	Default settings	--	800	--	mV
V_{FBUV}	Trim pin under-voltage threshold	Default settings	--	528	--	mV
$V_{UVOV(acc)}$	Trim UV/OV accuracy over range		-4	--	4	%
Note: The reference voltage of Trim is 600mV. Before the Trim voltage reaches 800mV, the product will turn off the drive but not enter the overvoltage protection state (latch off). After the Trim voltage reaches 800mV, the product latch off will be turned off.						
PGOOD						
V_{FBPGH}	PGOOD high threshold	Default settings	--	642	--	mV
V_{FBPGL}	PGOOD low threshold	Default settings	--	558	--	mV
$V_{PG(acc)}$	PGOOD accuracy over range		-4	--	4	%
$V_{PG(hyst)}$	PGOOD hysteresis voltage		15	28	45	mV
R_{PGOOD}	PGOOD pull-down resistance	V_{FB}=0V, I_{PGOOD}=5mA	--	50	--	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	V_{Trim} = 600 mV, V_{PGOOD} = 5 V	--	--	20	uA

$t_{PGDELAY}$	PGOOD delay time after soft-start sequence is complete	Default settings	--	2	--	ms

General Specifications

Item	Operating Conditions	Min.	Typ.	Max.	Unit
Operating Temperature	See temperature derating curve	-40	--	85	℃
Storage Temperature		-55	--	125	
Storage Humidity	Non-condensing	5	--	95	%RH
Reflow Soldering Temperature*		Peak temperature Tc≤245℃, the maximum time above 217℃ is 60 s			
MTBF	MIL-HDBK-217F@25℃	13869	--	--	k hours
Altitude		--	--	2000	m
Vibration		10-150Hz, 5G, 0.75mm. along X, Y and Z			
Moisture Sensitivity Level (MSL)	IPC/JEDEC J-STD-020D.1	MSL 3			
Pollution Degree		PD 3			

Note: * For actual application, please refer to IPC/JEDEC J-STD-020D.1.

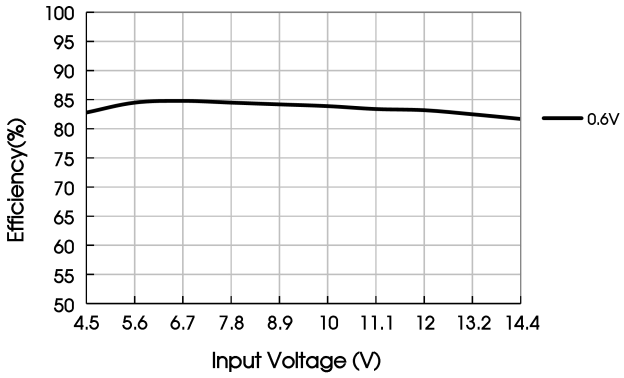
Mechanical Specifications

Case Material	Open frame
Dimensions	33.03 x 13.46 x 10.60 mm
Weight	13.2g
Cooling Method	Free air convection or forced convection

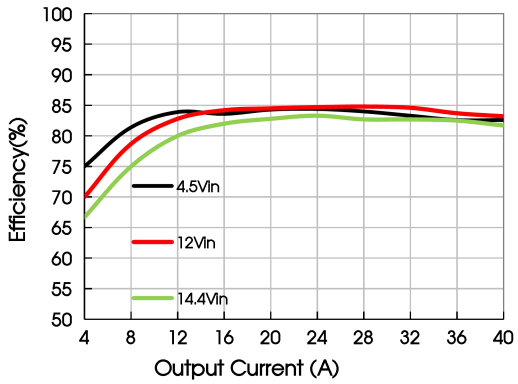
Typical Performance Curves

The following diagram provides a typical characteristic curve (0.6V output, 25℃).

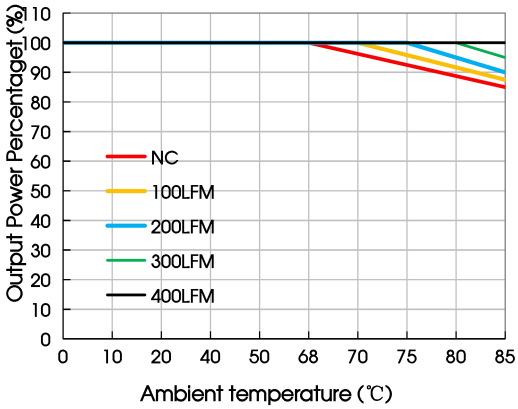
Efficiency Vs Input Voltage (Full Load)

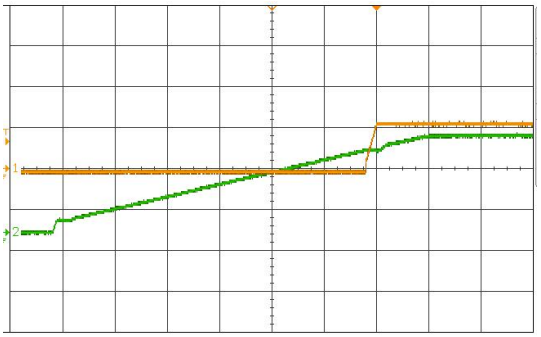


Efficiency Vs Output Load(Vout=0.6V)

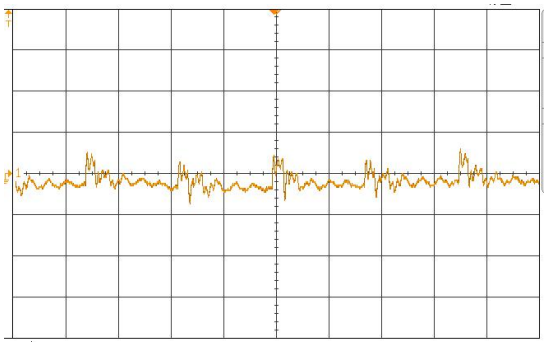


Temperature Derating Curves（Vo=0.6V）

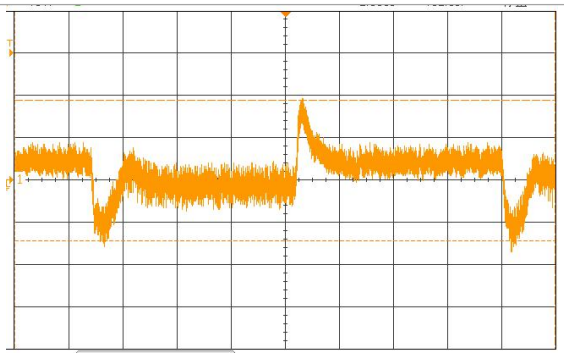




Green: input voltage, Yellow: output voltage (500mV/div), time(10ms/div)

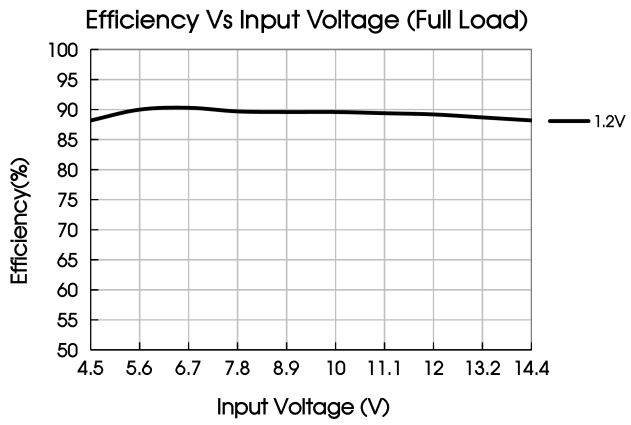


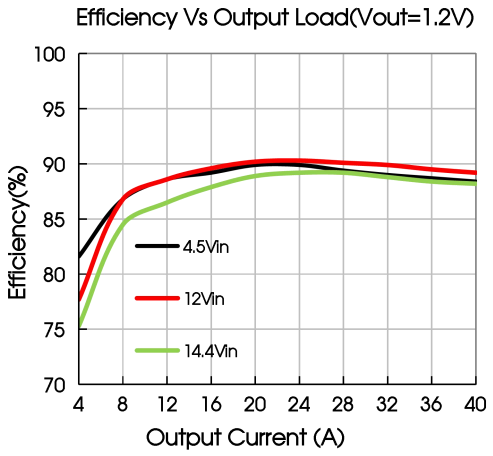
Output ripple & noise(5mV/div), Bandwidth: 20MHz

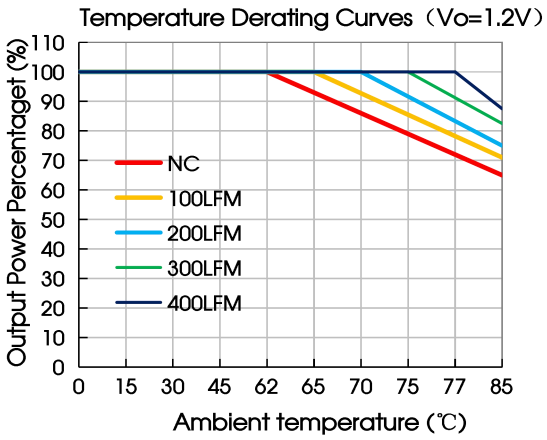


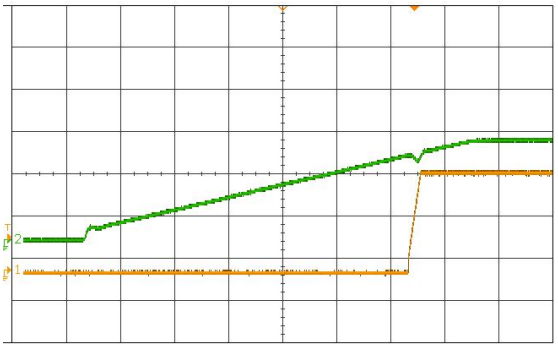
Output Transient Response (10mV/div), 100A/us, 10A-30A-10A, Bandwidth: 20MHz

The following diagram provides a typical characteristic curve (1.2V output, 25℃).

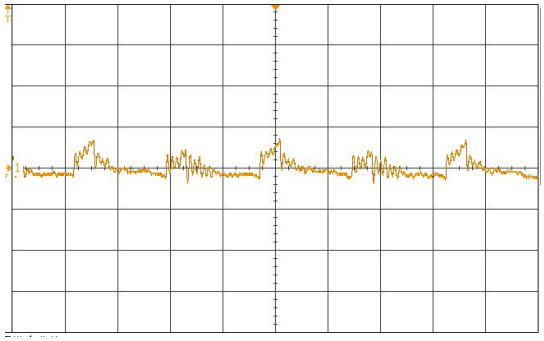




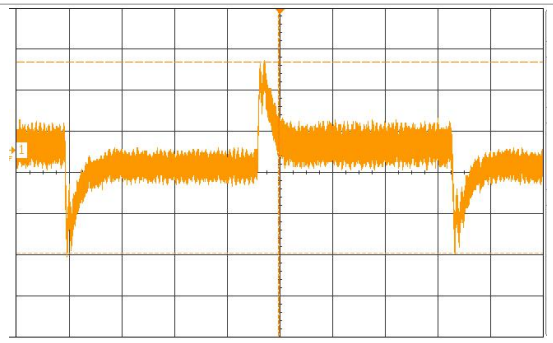




Green: input voltage, Yellow: output voltage (500mV/div), time(10ms/div)

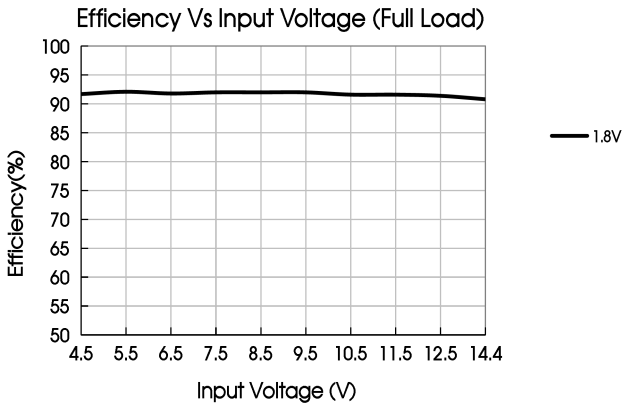


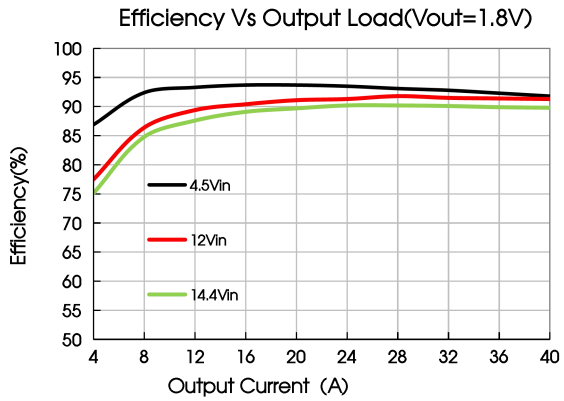
Output ripple & noise(10mV/div), Bandwidth: 20MHz

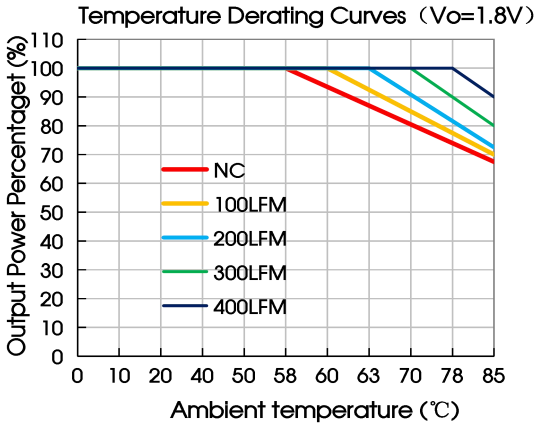


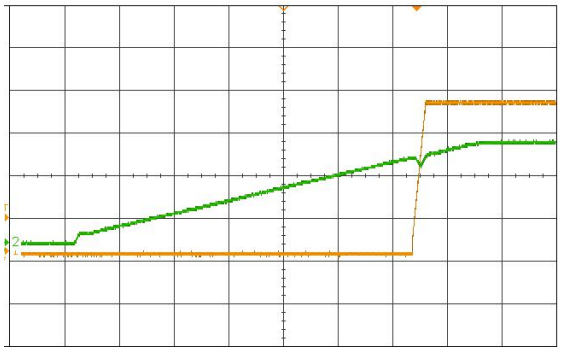
Output Transient Response (10mV/div), 100A/us, 10A-30A-10A, Bandwidth: 20MHz

The following diagram provides a typical characteristic curve (1.8V output, 25℃).

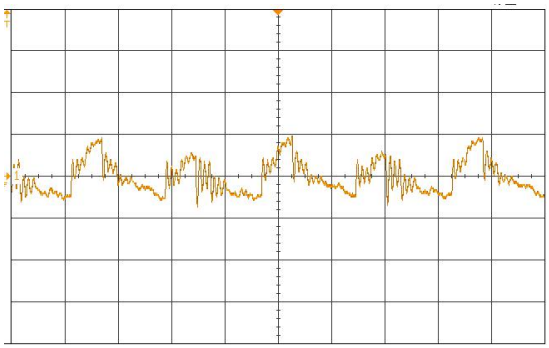




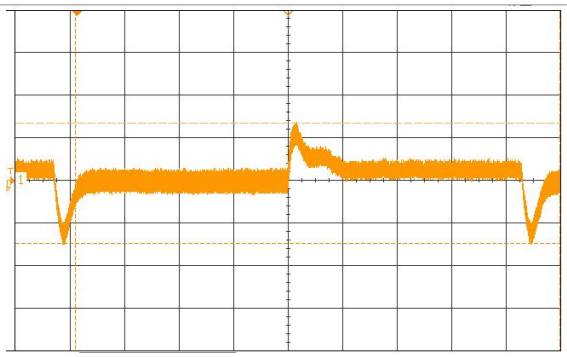




Green: input voltage, Yellow: output voltage (500mV/div), time(10ms/div)



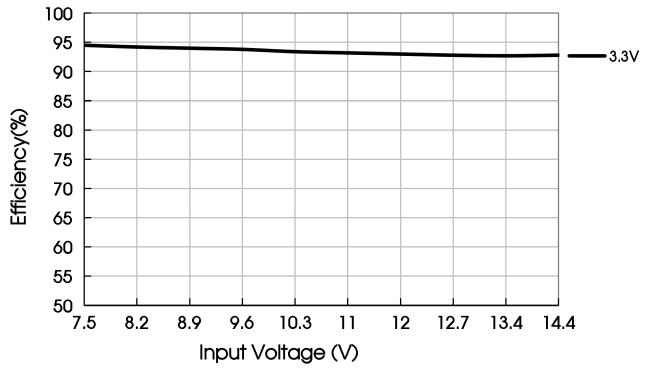
Output ripple & noise(10mV/div), Bandwidth: 20MHz



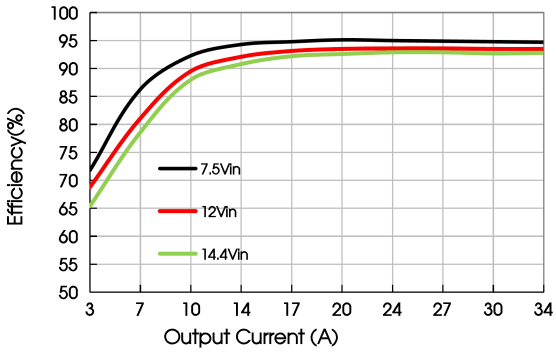
Output Transient Response (20mV/div), 100A/us, 10A-30A-10A, Bandwidth: 20MHz

The following diagram provides a typical characteristic curve (3.3V output, 25℃).

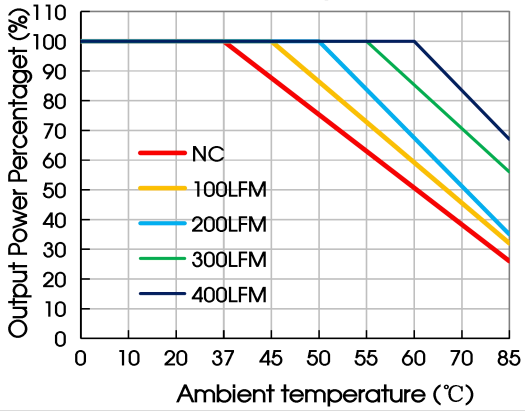
Efficiency Vs Input Voltage (Full Load)

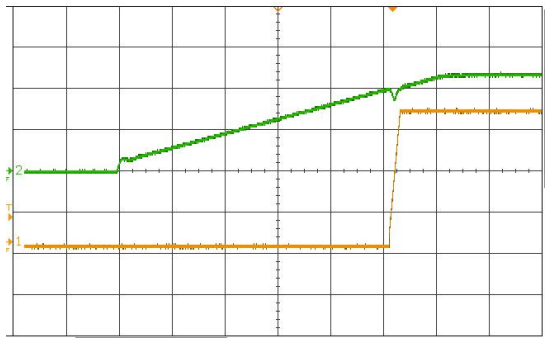


Efficiency Vs Output Load(Vout=3.3V)

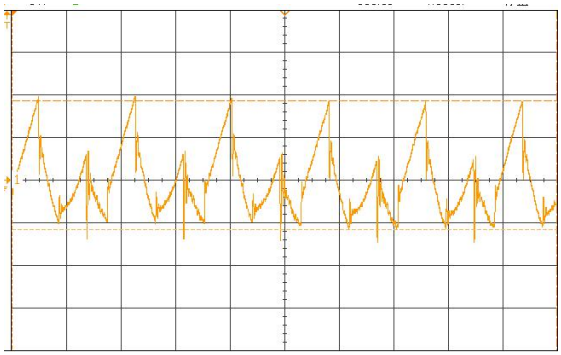


Temperature Derating Curves（Vo=3.3V）

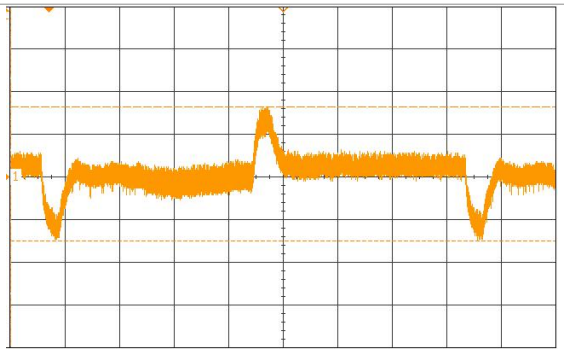




Green: input voltage, Yellow: output voltage (1000mV/div), time(11.6ms/div)

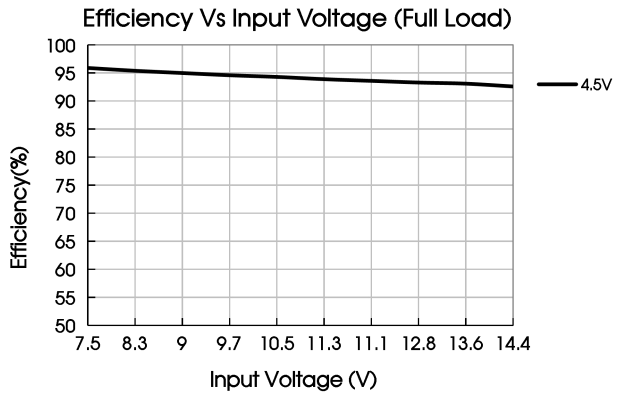


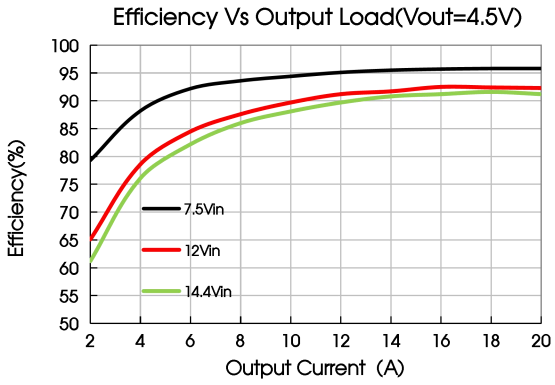
Output ripple & noise(10mV/div), Bandwidth: 20MHz

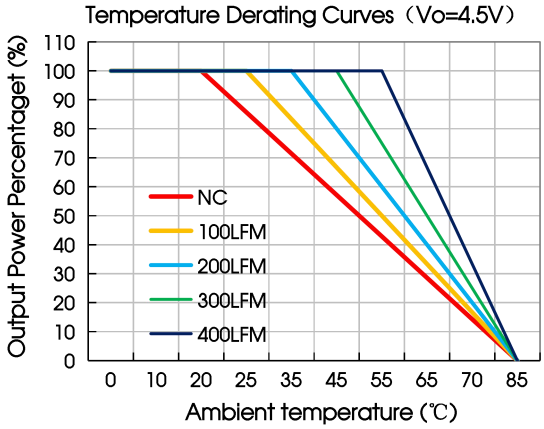


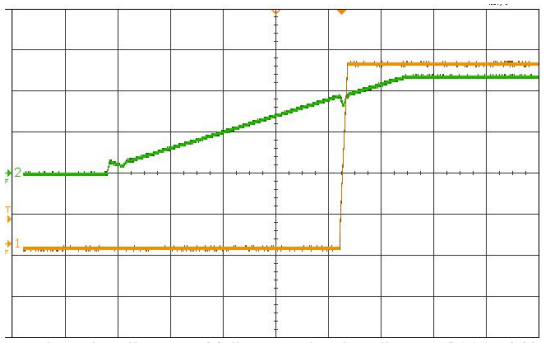
Output Transient Response (20mV/div), 100A/us, 8.5A-25.5A-8.5A, Bandwidth: 20MHz

The following diagram provides a typical characteristic curve (4.5V output, 25℃).

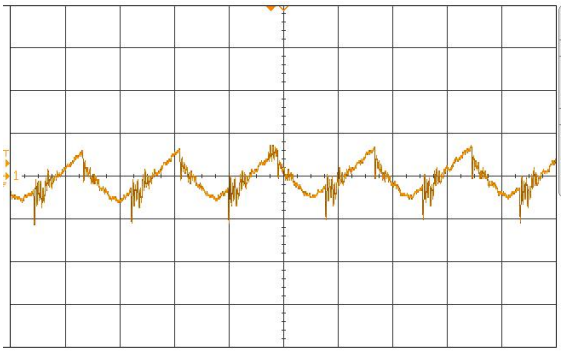




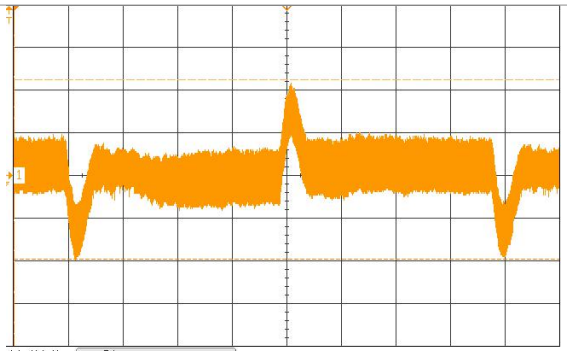




Green: input voltage, Yellow: output voltage (1000mV/div), time(16.4ms/div)



Output ripple & noise(10mV/div), Bandwidth: 20MHz



Output Transient Response (20mV/div), 100A/us, 5A-15A-5A, Bandwidth: 20MHz

Input Filtering

The module should be connected to a low ACR power supply. An input capacitor must be ensured near the input pin of the module to ensure the stability of the module. To minimize input voltage ripple, ceramic capacitors with ESR and electrolytic/polymer capacitors with low ESR are recommended.

If applied to 4.5V input applications, please follow the following suggestions:

a. The input voltage of the front stage must be ≥ 4.5V;

B. Recommended for front-end PCB layout: It is recommended to use at least 4oz, width greater than 1cm, length less than 5cm.

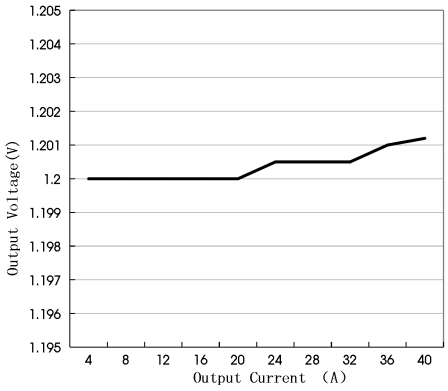
Output Ripple & Noise

The default loop compensation can be adapted to most application requirements. In addition, the output of the product will have some low-frequency ripple interference, which has nothing to do with the instability of the control loop. The total output ripple and noise of the module can be kept at a low amplitude.

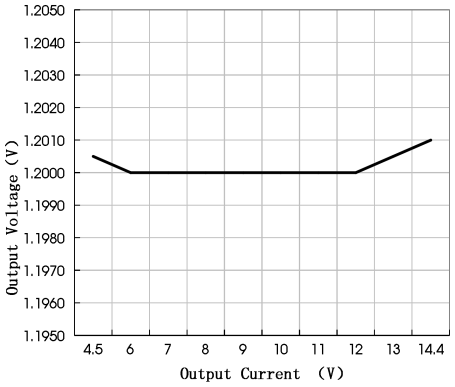
It is recommended to place ceramic capacitors with low ESR and electrolytic/polymer capacitors with low ESR as close to the load as possible and parallel multiple capacitors to lower their ESR. To make capacitors more effective, it is recommended to pay attention to PCB layout and wiring when applying.

Output Accuracy

This module is a high-precision product. The output current is 0-40A, the output voltage is 1.2VDC, and the input is 4.5-14.4VDC. The typical accuracy curve is:



Load adjustment deviation



Linear adjustment deviation

PMBus Data Format

PMBus data format

The PMBus command (set threshold, voltage, or exception status) supports three data formats that require literal and numeric representations as parameters (set threshold, voltage, or report such commands). Compatible modules need to support only one of these formats. Modules support only linear data formats for these commands. In this format, the data parameter consists of two parts, mantissa and exponent. The number represented by this parameter can be expressed as:

$$Value = mantissa \times 2^{exponents}$$

PMBus Address

On the bus, each PSU must be assigned a unique ADDRESS. 64 addresses (0-63) can be selected through the ADDRESS 1 and ADDRESS 0 pins. The addresses are set in the form of two octal (0-7) digits (0 to 63 in decimal notation), one number per pin. ADDRESS 0 is a low order number. During PMBus communication, PMBus ADDRESS bit '0b' +ADDRESS 1+ADDRESS 0 of the module power supply, and the address setting resistance is shown in the following table:

number	resistance(kΩ)
0	8.45
1	16.2
2	25.5
3	37.4
4	54.9
5	84.5
6	133
7	200

Such as:
ADDRESS 1 uses a 37.4K resistor, ADDRESS 0 uses a 37.4K resistor, and the octal value is 33. The actual bit machine displays 27 address bits.

Note:
1. If the pin resistances of ADDRESS 1 and ADDRESS 1 are out of range, the power module will not continue to respond to PMBus instructions, and the upper computer will not show that the module is detected;
2. Other resistance values may cause incorrect PMBus addresses. You are advised to ensure that the resistance values are consistent with the preceding table.

Module Startup and Shutdown

The startup and shutdown of the module are jointly controlled by the PMBus Operation instruction, remote Control pin and input voltage.

Note:

If the module is running within the shutdown delay time, avoid opening the module before the shutdown delay time expires. The module is allowed to open only after the shutdown delay time has ended and the module has been turned off. This is also true for applications where two modules are in parallel, the switch delay time of both modules must be configured to the same value.

Soft Start

The soft start up time of the module can be configured. The TON_RISE PMBus command is optional from 600 us to 9 ms. For details, see the command description. When selecting the soft start time, the charging current on the output capacitor should be considered. In applications with a large number of output capacitors, this current will lead to over current protection and shut down the module. Therefore, in order to ensure that these problems do not occur, the charging current of the output capacitor should be considered when considering the setting of the over current threshold.The charging current of the output capacitor can be obtained by the following formula:

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}}$$

•ICAP is the charging current of the output capacitor (unit: A)

•VOUT is the output voltage of the module, expressed in V

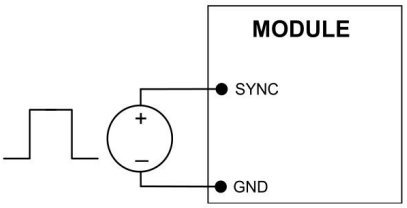
•COUT is the total capacity of the output capacitance, expressed in F

•tSS indicates the selected soft start up time (unit: s)

After calculating the charging current, the over current threshold can be configured as the sum of the maximum load current and the charging current of the output capacitor with a certain margin. The margin required can depend on the particular application, but 25% is recommended.

Note:
When two modules are connected in parallel, the soft start up time of the two modules must be the same.

Set Frequency and Synchronize Clock



The switching frequency of a module can be synchronized to a signal with an external frequency within a specified range. Add an external clock signal to the SYNC pin of the module as shown in the figure above. The external clock must meet the requirements of the external SYNC signal specified in the electrical specification table.

If this pin is not used, the module should run at the default switching frequency and connect the SYNC pin to GND.

The switching frequency can be synchronized using an external clock on the SYNC pin. When two modules work in parallel, the SYNC signal frequency must be 4 times the switching frequency, and the SYNC signal must be a square waveform with a duty cycle of 50%. The high level threshold should be greater than 2V and the low level threshold should be less than 0.8V. Changes to SYNC and SHARE2 Settings take effect only after the power is restarted.

On-off Delay

The startup delay time, output voltage rise time and shutdown delay time can be set through the upper computer. More information can be consulted in the PMBus instruction.

Output Voltage Setting

The TRIM pin is connected to the input of the internal error amplifier with an internal reference voltage of 600 mV±0.5%.

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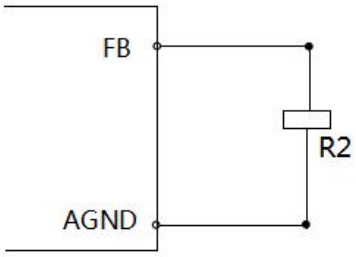

VO(SET)	resistance(kΩ)
0.6	OPEN
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10
3.3	4.4444
4.5	3.0791

$$R2 = R_{FBX}(k\Omega) = \frac{6}{V_O - V_{FB}}$$

The module's output voltage can be adjusted using the MFR_SPECIFIC_04 (VREF_TRIM) (D4h) command, which is formatted in a specific_mfr_specific_04 (VREF_TRIM) (D4h) command. It is adjusted between -20% and 10% of the output voltage. Step by 2mV. In addition, MARGINING and VREF_TRIM limit the output voltage adjustable range to -30% to 10%, and it is not recommended to exceed this range.

KD12T-40A can determine the actual output voltage through the following three forms:

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KD12T-40A can determine the actual output voltage through the following three forms:

- No output margin

$$V_{FB} = VREF\_TRIM + 0.6$$

- Margin High Voltage State

$$V_{FB} = STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM + 0.6$$

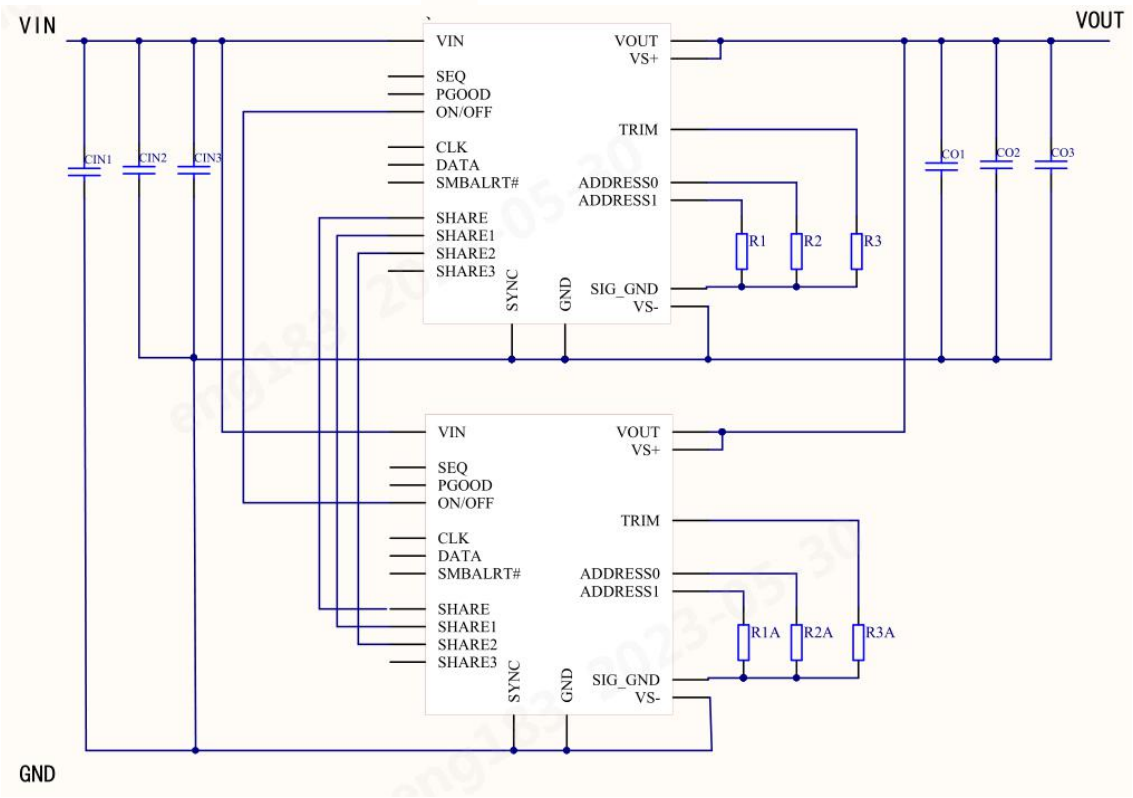
- Margin Low State

$$V_{FB} = STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM + 0.6$$

- VTRIM is the voltage on the TRIM pin
- VREF_TRIM is the offset voltage of the output voltage
- VREF_MARGIN_HIGH is the upper limit of marginal voltage where the output voltage is adjustable
- VREF_MARGIN_LOW is the lower limit of marginal voltage where the output voltage is adjustable

Multi-module Parallel Application

The module can support multi-module parallel application, with a maximum of two modules in parallel to 80A. The connection mode is as follows:



Note:

The SH pins must be connected together to ensure that the current is shared among channels. The SHARE1 pin requires the bus to be connected together to ensure that all channels are closed in the event of any channel failure. You also need to ensure that the MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h) command is configured correctly to ensure the correct phase shift between the phases of each channel. The SYNC pins of the two modules need to be connected to the bus, and the SHARE2 pins of the two modules need to be connected to the bus to ensure phase shift.

The upper computer Settings are as follows:

Two-module configuration	Main module			Slave module		
	SYNC-MODE	ENSYNC	PHASE	SYNC-MODE	ENSYNC	PHASE
	00	①	11	11	①	11

① Perform the following operations to configure the two modules to avoid potential damage.

1. Set ENSYNC to 0 in each module;

2. Set SYNC-MOD and PHASE correctly on the two modules, save them in EEPROM, and restart the module;

3. Set ENSYNC to 1 for each module to ensure that the synchronization function is enabled for the two modules without restarting the module.

Note:

1. In the parallel mode of two modules, the SHARE3 and ISH pins must be connected to the bus to ensure the equal flow between channels, and the SHARE1 pin must be connected to the bus to ensure that the fault information of each channel can be shared.We also need to ensure that the MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h) instruction is set correctly to ensure proper phase between channels. We also need to ensure that SHARE2 pins are connected to the bus to ensure phase interleaving.
2. Ensure that the start up time of the two modules is the same. For details, see the PMBus Operation Guide.
3. SYNC of the two modules must be connected to ensure that the two modules have the same frequency;
4. SYNC-MODE, ENSYNC, and PHASE are the name of the upper computer register module;
5. Cloth board recommendation; The product is designed with more signal lines, and the signal lines between modules are as short as possible to reduce parasitic capacitance;
6. For SHARE3, if follow the diagram connection method, it can ensure that current sharing between the two modules, otherwise please do not connect.

PGOOD

The module will detect the voltage on the TRIM pin to determine whether the output voltage is within the set value range. During the soft start, PGOOD is pulled to the ground. After the soft start, if the output voltage is within the PGOOD threshold range (PG_LOW to PG_HIGH), the PGOOD pin will be released after a delay of 2ms. When the output voltage is beyond the PGOOD threshold range, PGOOD will be pulled to the ground immediately. The PGOOD threshold range (PG_LOW and PG_HIGH) can be set using the PMBus directive MFR_SPECIFIC_07(PCT_VOUT_FAULT)PG_LIMIT.

PGOOD is leak-opening pin, which needs external 10K resistance;

Output over-current Protection

Output over-current protection, the upper computer can set two response modes, one is self-recovery from short circuit, and the other is module latch after short circuit. The short circuit period is 7 cycles (7 x module output voltage rise time). When two modules are applied in parallel, the over-current protection response of the two channels follows the over-current protection response of the one channel. The two modules must be set in the same over-current protection response mode.

VOUT UV/OV

The module detects the voltage on the TRIM pins and is used to provide output over-voltage and output under-voltage protection. Both the output over-voltage and output under-voltage thresholds can be set on the PMBus instruction. Output under-voltage protection works in the same way as over-current protection,

For example, if the IOUT_OC_FAULT_RESPONSE command sets the response to a self-restoring restart, the under-voltage protection response will also be a self-restoring restart. In addition, the under-voltage protection will not detect until the soft boot is complete.

When the output over-voltage protection fault occurs, until the power is restarted or the CNTL is switched over.When the output over-voltage threshold is set to a percentage of the output voltage, the output over-voltage protection is enabled only after the soft boot is complete. When the output over-voltage threshold is set to a fixed value, the output over-voltage protection takes effect continuously. In parallel applications, ensure that the connection of SHARE1 of the two modules to SHARE1 bus only detects the output under-voltage/over-voltage fault of TRIM1 of module 1 (host), and other channels are not detected. For more information, see

MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h) and (E0h).

MFR_SPECIFIC_16 (COMM_EEPROM_SPARE) instruction.

VIN UV

Input under-voltage protection can also be set through the upper computer. For details, please refer to VIN_ON and VIN_OFF instructions. The default under-voltage is described in the electrical performance table.

OT

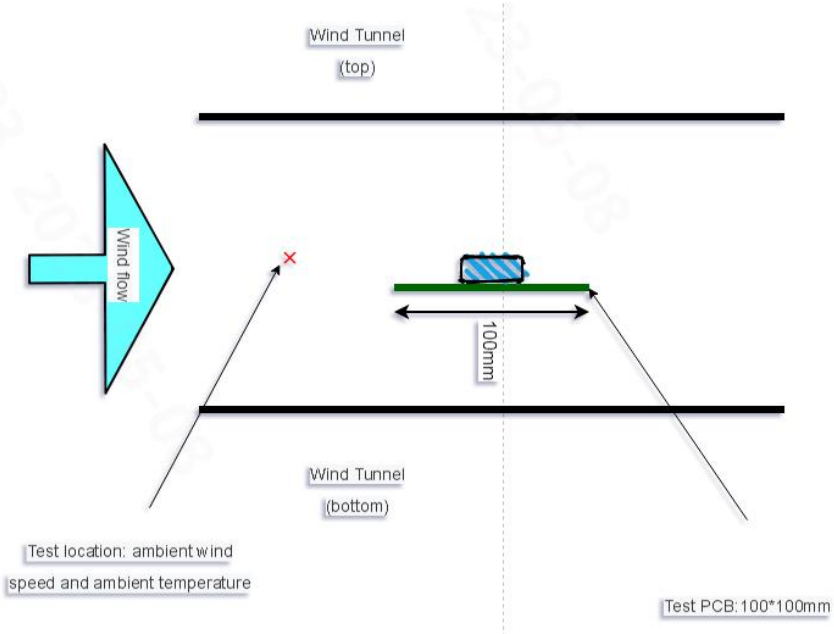
The module has protection function inside. The upper computer can modify the over-temperature protection point synchronously, which can be set between 120℃ and 160℃.

When the internal control IC over-temperature fault (160℃), the PWM of the control IC is turned off. When the temperature drops to 140℃, the PWM restarts.

Thermal Design

The product can operate in different thermal environments, but sufficient heat dissipation must be provided to ensure reliable module operation. Heat dissipation is mainly realized through the heat conduction from the module pins to the main board and the convective wind speed flowing through the module. The product has a certain degree of derating, but it is not recommended to use over-temperature. The temperature derating curve provides the relationship between the output current and the ambient temperature and wind speed under a specific Vin. See the above table for details.

The module was tested on a 100 x 100mm test plate, installed vertically in a wind tunnel with a cross section of 300 x 203 mm. Also note that the low impedance of the connection between the module and the motherboard effectively reduces the additional power loss.



SHARE1 Fault information

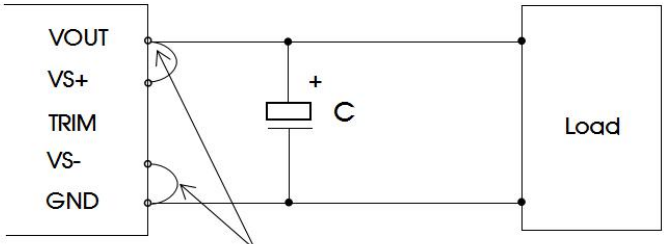
The SHARE1 pin will be pulled down internally when triggering an over-current, input under-voltage, output over-voltage, output under-voltage, and over-temperature failure. In addition, if the SHARE1 pin of the module is pulled down externally, the module will also shut down.

If the fault response is set to self-recovery, SHARE1 can only be restarted after each channel has been released.

Fault information	Input under-voltage	Over current	Output voltage Under shoot	output over voltage	over-temperature
Response model	/	Self-recovery or latching can be set	Self-recovery or latching can be set	Latch	The temperature recovers automatically when it is lower than the enable threshold
Pre-soft start up	Turn on	Turn off	Turn off	Enable when the threshold is a fixed value or disable when the threshold is a percentage of the output voltage	Turn on
Soft boot	Turn on	Weekly term flow	Turn off	Enable when the threshold is a fixed value or disable when the threshold is a percentage of the output voltage	Turn on
After soft boot	Turn on	Turn on	Turn on	Turn on	Turn on

Use of Remote Compensation and Matters Needing Attention

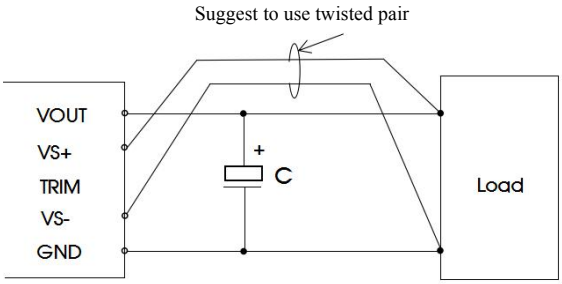
1, Remote Sense Application：



The line must be kept as short as possible

Note:
1) When no remote compensation is used, ensure that VOUT and VS+, GND and VS- are short connected;
The cable between VOUT and VS+ and GND and VS- should be as short as possible and close to the terminal. Avoid the formation of a large loop area, when noise into this loop, may cause instability of the module.

2, Remote Sense Connection used for Compensation：

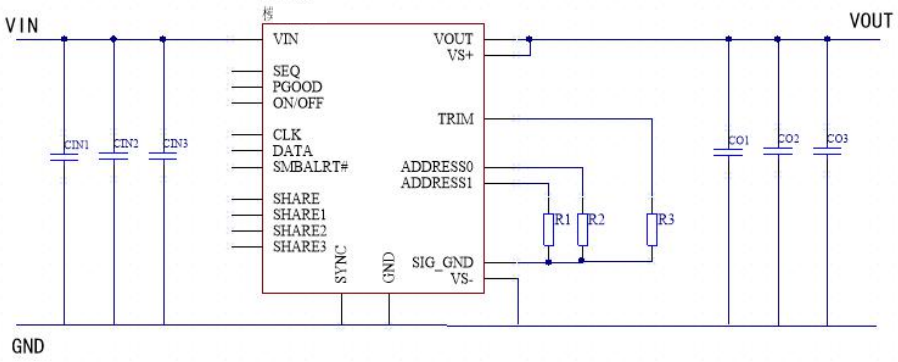


Note:
1. If a long remote compensation lead is used, the output voltage may be unstable. If a long remote compensation lead must be used, contact our technical personnel.
2. If remote compensation is used, use twisted pair cables or shielded cables and make the leads as short as possible.
3. Use wide PCB leads or thick wires between the power module and the load, and keep the line voltage drop lower than 0.3V. Ensure that the output voltage of the power module is within the specified range.
4. The impedance of the lead may cause output voltage oscillation or large ripple. Please make adequate evaluation before use.

Design Reference

Application circuit

Components	Recommended Component Value
CIN1	470uF/25V electrolytic capacitor
CIN2	3*22uF/25V ceramic capacitor
CIN3	0.1uFuF/25V ceramic capacitor
CO1	0.1uFuF/6.3V ceramic capacitor
CO2	5*47uF/6.3V ceramic capacitor +2*22uF/10V ceramic capacitor
CO3	4*100uF/50V+1*680uF/35V electrolytic capacitor
R1	OPEN
R2	
R3	20K



Recommended typical application:

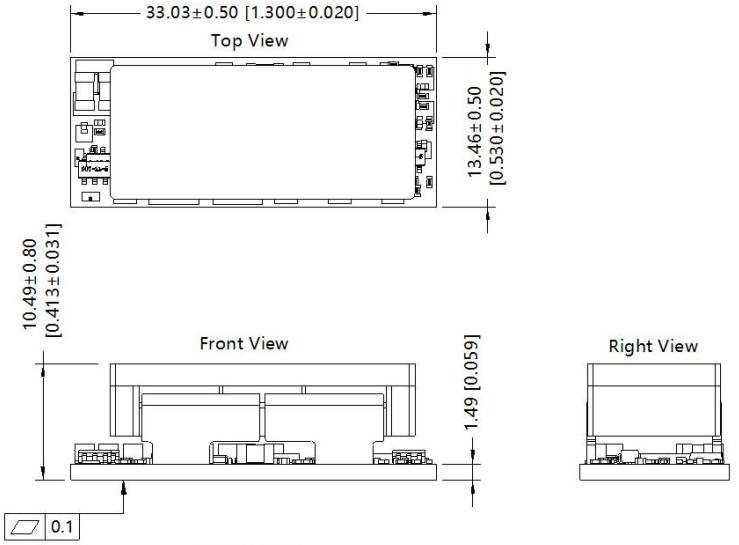
VIN: 12V

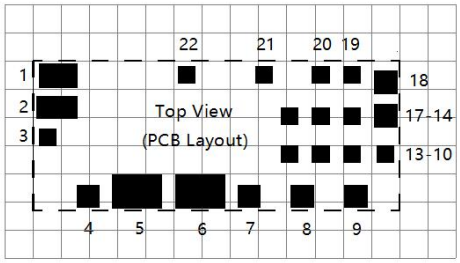
VOUT: 1.2V

IOUT: 40A

Dimensions and Recommended Layout

THIRD ANGLE PROJECTION

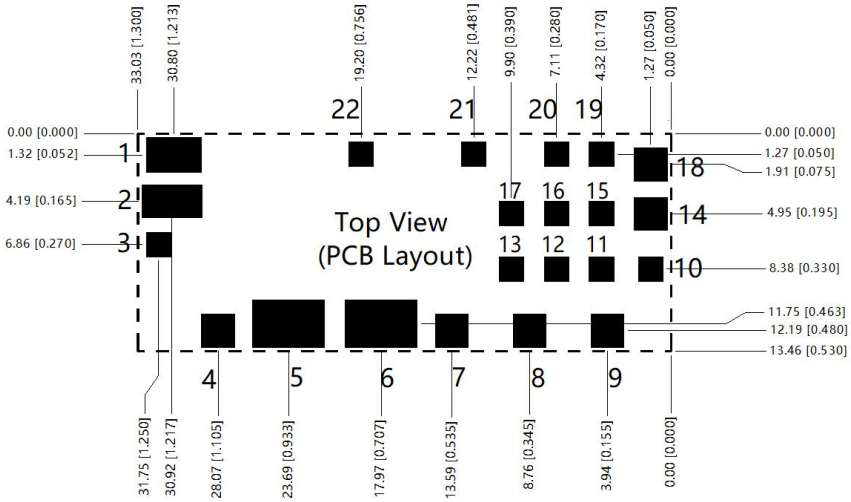


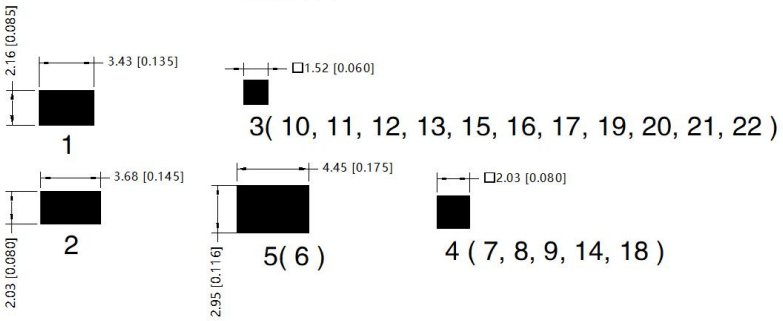


Note: Grid 2.54*2.54mm

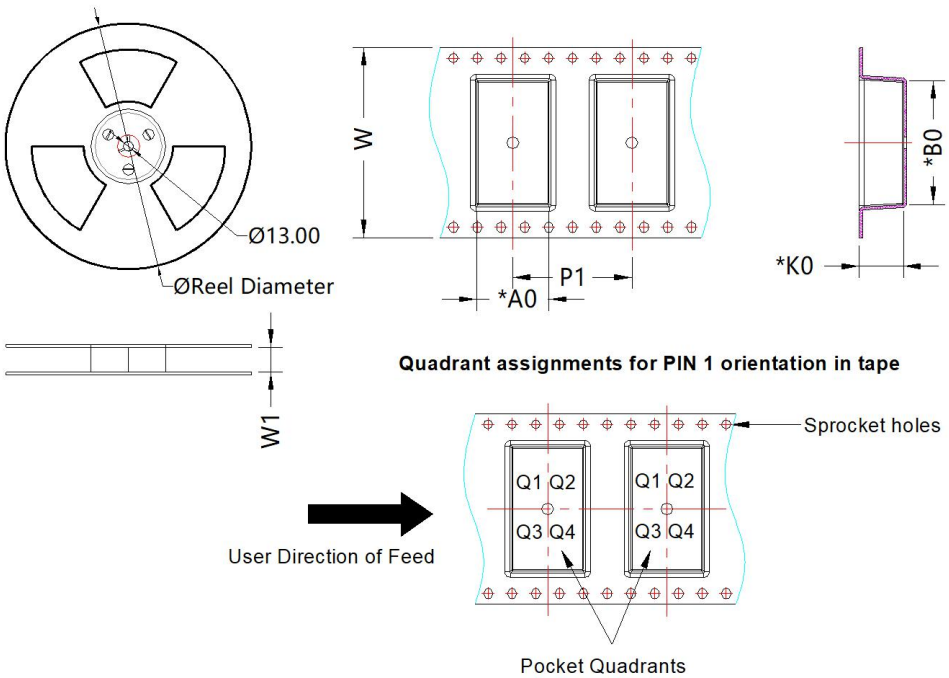
Note:
Unit: mm[inch]
General tolerances: ±0.25[±0.010]
The layout of the device is for reference only, please refer to the actual product

Pin-Out			
Pin	Mark	Pin	Mark
1	Vin	12	DATA
2	GND	13	SHARE1
3	SYNC	14	GND
4	NC	15	SIG_GND
5	GND	16	SHARE2
6	Vo	17	SHARE3
7	Trim	18	ON/OFF
8	GND	19	ADDRESS 1
9	SHARE	20	ADDRESS 0
10	VS-	21	SMBALERT#
11	CLK	22	PG





Packaging Details



Device	Package Type	Pin	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
KD12T-40A	SMD	22	190	330.0	56.4	14.6	34.21	12.04	24	56	Q2

PMBus Key Register Details

OPERATION(01h)	This instruction is used to operate CNTL (ON/OFF) to turn the module on or off. It can also be used to set the fine setting of the output voltage. The OPERATION of channel 1 register to access the module, PAGE must be set to 0, if the OPERATION of channel to access the module 2 registers, PAGE must be set to 1, if you want to access the channel 1 and channel 2 at the same time, the PAGE must be set to 11. If the channel is configured to machine, the channel can't access the directive, the directive of any written will be ignored, try to read and write any instruction from machine channel will report the fault and trigger SMBALERT.
IOUT_CAL_GAIN	IOUT_CAL_GAIN must equal the actual inductor DCR value to achieve accurate current reading and OC failure protection.
Enable and UVLO	The ON_OFF_CONFIG command is used to select the enable behavior of the converter. In this case, as long as there is the input voltage and higher than the UVLO threshold, whatever state of operations, all use ON/OFF terminal to enable or disable the converter. If the ON/OFF terminal dangling through internal 6 mu A current source pull it to 5 v.
TON_RISE	Soft start up time Command to set the soft start time. The charging current of the output capacitor should be considered when selecting the soft start time. In some applications (for example, has a large number of output capacitance application), if not properly choose soft start time, then the current may result in wrong jump over current protection circuit.In order to avoid the mistake of jump, when choosing soft start time and over current output capacitor charging current threshold should be included. You can use the formula $I_{CAP} = \frac{V_{OUT} \times C_O}{t_{ss}}$ calculate the charging current of the capacitor.
IOUT_OC_FAULT_LIMIT	over-current threshold and response order over-current threshold can be set. The module uses the peak current value of the inductor for over-current detection. The current limit should be set to the maximum peak inductor current, plus the output capacitor charging current during start up, plus some load transients and allowance for component changes. The amount of margin required depends on the individual application, for which the maximum peak inductor current is, the design allows for some additional margin, so an over-current threshold of 50A (peak current) is chosen.
IOUT_OC_FAULT_RESPONE	The IOUT_OC_FAULT_RESPONE command sets the desired overflow event response. In this example, the converter is configured to enter discontinuous mode when an over-current situation occurs. The module can also be configured to latch in the event of an over-current.

PMBus Detail Register

CODE	COMMAND NAME	WORD/BYTE	DESCRIPTION: PMBus Command	USER WRITABLE	FACTORY DEFAULT VALUE
00h	PAGE	Byte	Locates separate PMBus command lists in multiple output environments	YES	0XXX XXX0
01h	OPERATION	Byte	Turn the unit on and off in conjunction with the input from the CONTROL pin. Set the output voltage to the upper or lower MARGIN VOLTAGES.	YES	0X00 00XX
02h	ON_OFF_CONFIG	Byte	Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	YES	XXX1 0110
03h	CLEAR_FAULTS	Byte	Clears all fault status registers to 0x00. The "Unit is Off" bit in the status byte is not cleared when this command is issued.	YES[1]	NONE
10h	WRITE_PROTECT	Byte	Prevents unwanted writes to the device.	YES	000X XXXX
15h	STORE_USER_ALL	Byte	Saves the current configuration into the User Store. Note: This command writes to Non-Volatile Memory.	YES[1]	NONE
16h	RESTORE_USER_ALL	Byte	Restores Store. all parameters to the settings saved in the User	YES[1]	NONE

19h	CAPABILITY	Byte	PEC,SPD,ALRT	No	1011 0000
20h	VOUT_MODE	Byte	Read-Only Mode Indicator. The data format is linear with an exponent of -9	No	0001 0111
35h	VIN_ON	Word	Sets the value of the input voltage at which the unit should start power conversion	YES	1111 0000 0001 0001
36h	VIN_OFF	Word	Sets the value of the input voltage at which the unit should stop power conversion.	YES	1111 0000 0001 0000
38h	IOUT_CAL_GAIN	Word	Sets the ratio of the voltage at the current sense pins to the sensed current.	YES	1000 0000 0010 0001
39h	IOUT_CAL_OFFSET	Word	Nulls any offsets in the output current sensing circuit	YES	1110 0000 0000 0000
46h	IOUT_OC_FAULT_LIMIT	Word	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition.	YES	1111 1000 0001 1110
47h	IOUT_OC_FAULT_RESPONSE	Byte	Instructs the device on what action to take in response to an output over-current fault.	YES	0000 0111
4Ah	IOUT_OC_WARN_LIMIT	Word	Sets the value of the output current that causes an output Over-current warning	YES	1111 1000 0011 0010
4Fh	OT_FAULT_LIMIT	Word	over-temperature fault threshold	YES	0000 0000 1000 0010
5Ih	OT_WARN_LIMIT	Word	over-temperature warning threshold	YES	0000 0000 01111000
61h	TON_RISE	Word	Target soft-start rise time	YES	1110 0000 0010 1011
78h	STATUS_BYTE	Byte	Single byte status indicator	No	0x00 0000
79h	STATUS_WORD	Word	Full 2-byte status indicator	No	0000 0000 0x00 0000
7Ah	STATUS_VOUT	Byte	Output voltage fault status detail	No	0000 0000
7Bh	STATUS_IOUT	Byte	Output current fault status detail	No	0000 0000
7Dh	STATUS_TEMPERATURE	Byte	Temperature fault status detail	No	0000 0000
7Eh	STATUS_CML	Byte	Communication, memory, and logic fault status detail	No	0000 0000
80h	STATUS_MFR_SPECIFIC	Byte	Manufacturer specific fault status detail	No	0000 0000
8Bh	READ_VOUT	Word	Read output voltage	No	0000 0000 0000 0000
8Ch	READ_IOUT	Word	Read output current	No	1110 0000 0000 0000
8Eh	READ_TEMPERATURE_2	Word	Read off-chip temp sensor	No	1111 0000 0110 0100
98h	PMBUS_REVISION	Byte	PMBus Revision Information	No	0001 0001
D0h	MFR_SPECIFIC_00	Word	User scratch pad	YES	0000 0000 0000 0000
D4h	MFR_SPECIFIC_04	Word	VREF_TRIM	YES	0000 0000 0000 0000
D5h	MFR_SPECIFIC_05	Word	STEP_VREF_MARGIN_HIGH	YES	0000 0000 0001 1110
D6h	MFR_SPECIFIC_06	Word	STEP_VREF_MARGIN_LOW	YES	1111 1111 1110 0010
D7h	MFR_SPECIFIC_07	Byte	PCT_VOUT_FAULT_PG_LIMIT	YES	XXXX XX10
D8h	MFR_SPECIFIC_08	Byte	SWQUENCE_TON_TOFF_DELAY	YES	111X 000X
E0h	MFR_SPECIFIC_16	Word	COMM_EEPROM_SPARE	YES	1011 0001 xxxx x011
E5h	MFR_SPECIFIC_21	Word	IC options	YES	0111 1111 0000 0000

E6h	MFR_SPECIFIC_22	Word	PWM_OSC_SELECT	YES	0000 0000 0000 0001
E7h	MFR_SPECIFIC_23	Word	Paged and Common MASK_SMBALERT	YES	0000 0000 0000 0000
EFh	MFR_SPECIFIC_30	Word	Temperature offset	YES	1111 1000 0000 0000
F0h	MFR_SPECIFIC_32	Word	API options	YES	0000 0000 0000 0000
FCh	MFR_SPECIFIC_44	Word	Device code, unique code to id part number	No	0000 0001 1110 0000

NOTE 1：No data bytes are sent, only the command code is sent.

PAGE(00h)

Format	Unsigned binary integer
Description	The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs) of the device.
Default	0XXX XXX0 (binary)

PAGE							
r/w	r	r	r	r	r	r	r/w
7	6	5	4	3	2	1	0
PA	X	X	X	X	X	X	P0

Bits	Field Name	Description
7,0	PA,P0	00: (Default) All commands address the first channel. 01: All commands address the second channel. 10: Illegal input-ignore this write, take no action. 11: All commands address both channels. If PAGE = 11, any then read commands point to PAGE0 always.
6:1	X	X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

OPERATION (01h)

Format	Unsigned binary integer
Description	The OPERATION command is used to turn the device output on or off in conjunction with the input from the CNTLx pin (where x = 1 for channel 1 and x = 2 for channel 2). It is also used to set the output voltage to the upper or lower MARGIN levels. OPERATION is a paged register. In order to access OPERATION register for channel 1 of the device, PAGE must be set to 0. In order to access OPERATION register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0X0000XX (binary)

r/w	r	r/w	r/w	r/w	r/w	r	r
7	6	5	4	3	2	1	0
On	0	Margin				X	X

Bits	Field Name	Description
7	On	The On bit is used to enable to IC via PMBus. The necessary condition for this bit to be effective is that the cmd bit in the ON_OFF CONFIG register is set high. However, the cmd bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit cpr in the ON_OFF CONFIG register is low, or c. The bit cpr is high and the CNTL_EN pin is enabled (high or low).
6	0	X: Default

5:2	Margin	If Margin Low is enabled, load the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, load the value from the STEP_VREF_MARGIN_HIGH command. (See PMBus specification for more information) 0000: (Default) Margin Off 0101: Margin Low (Ignore Fault) 0110: Margin Low (Act On Fault) 1001: Margin High (Ignore Fault) 1010: Margin High (Act On Fault) Note: Any values written to read-only registers are ignored.
1:0	X	XX: Default X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

ON_OFF_CONFIG (02h)

Format	Unsigned binary integer
Description	The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. ON_OFF_CONFIG is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. However, note that page 0 (channel 1) fault status bits (and associated smbalert state) should be capable of being cleared by toggling CNTL1 pin even if channel 1 is a slave. If channel 2 is a slave, then CNTL2 pin is disabled but toggling the CNTL1 pin should also clear page 1 (channel 2) fault status bits and related smbalert state. (The is recommendation is to tie together CNTL1 pins of both devices in a multi-phase configuration).
Default	XXX10110 (binary) The default power-up state can be changed using the STORE_USER_ALL command.

			r/w^E	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
X	X	X	pu	cmd	cpr	pol	cpa

Bits	Field Name	Description
7:5	X	X indicates writes are ignored and reads are 0.
4	pu	(Format: binary) Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and/or PMBus commands. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up. 0: Device powers up any time power is present regardless of state of the CONTROL pin. 1: (Default) Device does not power up until commanded by the CNTL_EN pin and/or OPERATION command as programmed in bits (3:0) of the ON_OFF_CONFIG register.
3	cmd	(Format: binary) The cmd bit controls how the device responds to commands received via the serial PMBus. This bit is used in conjunction with the 'cpr', 'pu', and 'on' bits to determine start up. 0: (Default) Device ignores the on bit in the OPERATION command. 1: Device responds to the on bit in the OPERATION command, as explained above.
2	cpr	(Format: binary) Set the CNTL_EN pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up. The cpr bit being high is a necessary but not sufficient condition to enable the IC via the CNTL_EN pin: 0: Device ignores the CNTL_EN pin, i.e., on/off is controlled only by the OPERATION command 1: (Default) The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, and the CNTL_EN pin is active (high or low), and b. The bit cmd in the ON_OFF CONFIG register is low, or c. The bit cmd is high and the bit on in the OPERATION register is high.
1	pol	(Format: binary) Polarity of the CONTROL pin 1: (Default) CONTROL pin is active high 0: CONTROL pin is active low To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect.

0	cpa	(Format: binary) Sets CONTROL pin action when commanding the unit to turn off. 0: (Default) Use the programmed turn-off delay. Note: Any values written to read-only registers are ignored on write and returns a '0' when read.

CLEAR_FAULTS (03h)

Format	N/A
Description	CLEAR_FAULTS is a paged command. In order to issue this command for channel 1 of the device, PAGE must be set to 0. In order to issue this command for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. At the same time, the device negates (clears, releases) its SMB_ALERT signal output if the device is asserting the SMB_ALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

WRITE_PROTECT (10h)

Format	N/A
Description	The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. Note: Valid setting of WRITE_PROTECT(7:5) bits disables the RESTORE_USER_ALL command' s ability to restore EEPROM data to protected PMBus Control/Status Registers (CSRs). However, an EEPROM (via the RESTORE_USER_ALL execution) restores the data to any registers the remain unprotected (either by a valid WRITE_PROTECT(7:5) setting, or by any invalid setting of these bits). No WRITE_PROTECT(7:5) bit setting affects the Reset-Restore operation. All registers having EEPROM support get updated. Likewise, STORE_USER_ALL command operation remains unaffected.
Default	000XXXXX (binary) The default power-up state can be changed using the STORE_USER_ALL command.

r/w^E	r/w^E	r/w^E					
7	6	5	4	3	2	1	0
bit7	bit6	bit5	X	X	X	X	X

Bits	Field Name	Description
7	bit7	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)
6	Bit6	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands. (bit5 and bit7 must be 0 to be valid data)
5	Bit5	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands. (bit6 and bit7 must be 0 to be valid data)
4:0	X	X indicates writes are ignored and reads are 0. Note: Any values written to read-only registers are ignored.
Invalid data written to WRITE_PROTECT(7:5) causes the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers to be set. INVALID DATA ALSO RESULTS IN NO WRITE PROTECTION (WRITE_PROTECT = 00h)!		

Data Byte Value	Action
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.

0100 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, and PAGE commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.

STORE_USER_ALL (15h)

Format	N/A
Description	Store all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the write operation with unpredictable memory storage results. It is recommended to turn the device output off before issuing this command. EEPROM programming faults set the cml bit in the STATUS_BYTE and the oth bit in the STATUS_CML registers.

RESTORE_USER_ALL (16h)

Format	N/A
Description	Write EEPROM data to those registers which: (1) have EEPROM support, and; (2) are unprotected according to current setting of the WRITE_PROTECT(7:5) bits. It is permitted to use the RESTORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn the device output off before issuing this command.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

CAPABILITY (19h)

Format	N/A
Description	This command provides a way for a host system to determine some key capabilities of this PMBus device.
Default	10110000 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
PEC	SPD		ALRT	Reserved			

Bits	Field Name	Description
7	PEC	(Format: binary) Packet Error Checking is supported. 1: Default Note: Any values written to read-only registers are ignored.
6:5	SPD	(Format: binary) Maximum supported bus speed is 400 kHz. 01: Default Note: Any values written to read-only registers are ignored.
4	ALRT	(Format: binary) This device does have a SMB_ALERT pin and does support the SMBus Alert Response Protocol. 1: Default Note: Any values written to read-only registers are ignored.
3:0	Reserved	Reserved bits. 0000: Default

VOUT_MODE (20h)

Format	N/A
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below.

	If a host sends a VOUT_MODE writer command, the device rejects the VOUT_MODE command, declare a communication fault for invalid data and respond as described in PMBus specification II section 10.2.2.
Default	00010111 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
Mode			Exponent				

Bits	Field Name	Description
7:5	Mode	(Format: binary) 000: (Default) Linear Format
4:0	Exponent	(Format: two's SHARE3 lement binary) 10111: (Default) Exponent value = - 9 Note: Any values written to read-only registers are ignored.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start power conversion assuming all other conditions are met.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4.25(default)	4.5	4.75	5	5.25	5.5	5.75
6	6.25	6.5	6.75	7	7.25	7.5
7.75	8	8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5	12	12.5
13	14	15	16			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data - in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_ON remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_ON should not attempt to set its value less than that of VIN_OFF.
Default	The default setting results in a real VIN_ON of 4.25 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11110 (bin) - 2 (dec) (equivalent LSB = 0.25 V) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the Mantissa for the linear format. Default: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Minimum: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Maximum: 000 0100 0000 (bin) 64 (dec) (equivalent VIN_ON voltage = 16 V) Note: Any values written to read-only registers are ignored

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop power conversion.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4(default)	4.25	4.5	4.75	5	5.25	5.5
5.75	6	6.25	6.5	6.75	7	7.25
7.5	7.75	8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25	11.75	12.25
12.75	13.75	14.75	15.75			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data – in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_OFF remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_OFF should not attempt to set its value equal to or higher than that of VIN_ON.
Default	The default setting results in a real VIN_OFF of 4 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) These default settings are not programmable. Note: Any values written to read-only registers are ignored
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the linear format Mantissa. Default: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Minimum: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Maximum: 000 0011 1111 (bin) 63 (dec) (equivalent VIN_OFF voltage = 15.75 V) Note: Any values written to read-only registers are ignored.

IOUT_CAL_GAIN (38h)

Format	Linear
Description	The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are ohms. The effective current sense element is the DCR of the inductor. The default setting is 0.5 mΩ. The resolution is 15.26 μΩ. The range is 0.244 to 7.747 mΩ. The IOUT_CAL_GAIN needs to be set to 0.5 mΩ for correct current readout. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1), PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE 0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. IOUT_CAL_GAIN is a paged register. In order to access this register for channel 1 of the device, PAGE(7), (0) must be set to 00. In order to access this register for channel 2 of the device , PAGE(7), (0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7), (0) command must be set to 11
Default	The default setting results in a real IOUT_CAL_GAIN of 0.5035 mΩ. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 10000 (bin) - 16 (dec) (15.26μΩ) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the linear format Mantissa. Default: 000 0010 0001 (bin) 32 (dec) (32×15.26μΩ = 0.5035 mΩ) Minimum 016 (dec) = 16×15.26 μΩ = 0.244 mΩ Maximum 508 (dec) = 508× 15.26 μΩ = 7.747 mΩ Note: Any values written to read-only registers are ignored.

IOUT_CAL_OFFSET (39h)

Format	Linear
Description	The IOUT_CAL_OFFSET is used to SHARE3ensate for offset errors in the READ_IOUT command, the IOUT_OC_FAULT_LIMIT command and the IOUT_OC_WARN_LIMIT command. The units are amps. The default setting is 0 A. The resolution is 62.5 mA. The range is 3.9375 A to -4 A. Values outside the valid range are not checked and become aliased into the valid range. For example, 1110 0100 0000 0001 has an expected value of–63.9375 A but results in 1110 0111 1111 0001 which is–3.9375 A. This change occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the mantissa are always equal to the sign bit. IOUT_CAL_OFFSET is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the controller, PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (i.e. the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value are used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11100 (bin) - 4 (dec) (lsb = 62.5 mA) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the linear format Mantissa. This is the linear format Mantissa. Default: 0 (bin) 0 (dec) Bits 1:0, and 7:6 changes for sign extension but are not otherwise programmable Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_LIMIT (46h)

Format	Literal
Description	The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should always be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the ' cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML registers and assert SMB_ALERT. IOUT_OC_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1000 0001 1110 (binary) The default setting results in a real IOUT_OC_FAULT_LIMIT of 30 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11111 (bin) -1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) Default: 000 0001 1110 (bin) 60 (dec) (equivalent analog OC = 30 A) Minimum: 000 0000 0110 (bin) 6 (dec) (equivalent analog OC = 3 A) Maximum: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_RESPONSE (47h)

Format	Unsigned binary
Description	The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT under-voltage (UV) fault. When an OC fault is triggered, the device also: • Sets the OCF bit in the STATUS_BYTE register • Sets the OCFW and OCF bits in the STATUS_WORD register • Sets the OCF and OCW bits in the STATUS_IOUT register • Asserts SMB_ALERT, and notifies the host as described in section 10.2.2 of the PMBus Specification.. Bits (2:0) are hard-wired to 0x7 (3'b111) to indicate the 7×Soft-start time delay units in response to an over current or Voutunder-voltage fault. IOUT_OC_FAULT_RESPONSE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK' d command and the reporting of an IVC fault and triggering of SMB_ALERT.

Default	0000 0111 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r/wE	r/wE	r/wE	r	r	r
7	6	5	4	3	2	1	0
0	0	RS(2)	RS(1)	RS(0)	1	1	1

Bits	Field Name	Description
7:6	0	Default: XX (X indicates writes are ignored and reads are 0) Note: Any values written to read-only registers are ignored.
5:3	RS(2:0)	(Format: binary) Output over current retry setting 000:(Default) A zero value for the Retry Setting indicates that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.). 111: A one value for the Retry Setting indicates that the unit goes through a normal startup (Wait → SoftStart) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000 or 111 is not accepted, such and attempt causes the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register to be set, and SMB_ALERT to be asserted.
2:0	1	Default: xxx (x indicates writes are ignored and reads are 1) Note: Any values written to read-only registers are ignored.

IOUT_OC_WARN_LIMIT (4Ah)

Format	Literal (5-bit two's SHARE3 lement exponent, 11-bit two's SHARE3 lement mantissa)
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition by setting the OCW in bit-5 of the STATUS_IOUT register. • Sets the OTHER bit in the STATUS_BYTE register • Sets the OCFW bit in the STATUS_WORD register • Set the OCW bit in the STATUS_IOUT register • Notifies the host (Asserts SMB_ALERT) IOUT_OC_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the K12DT-60A device, PAGE must be set to 0. In order to access this register for channel 2 of the K12DT-60A controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The IOUT_OC_WARN_LIMIT should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	1111 1000 0011 0010 (binary) The default setting results in a real IOUT_OC_WARN_LIMIT of 25 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/wE	r/wE	r/wE	r/wE	r/wE	r/wE	r/wE
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11111 (bin) - 1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.

2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the Mantissa for the linear format. Output over current retry setting Default: 000 0011 0010 (bin) 50 (dec) (analog OC Warning = 25 A) Minimum: 000 0000 0100 (bin) 4 (dec) (equivalent analog OC = 2 A) Maximum: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Note: Any values written to read-only registers are ignored.

OT_FAULT_LIMIT (4Fh)

Format	Literal (5-bit two's SHARE3 lement exponent, 11-bit two's SHARE3 lement mantissa)
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken: • Set the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Set the OTF and OTW bits in the STATUS_TEMPERATURE register • Notify the host (Asserts SMB_ALERT) • Generate internal signal/s CHx_TSD that eventually shut down the gate drivers. OT_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 10000010 (binary) The default setting results in a real OT_FAULT_LIMIT of 130° C. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1° C) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the Mantissa for the linear format. Default: 000 10000010 (bin) 130 (dec) (130° C) Minimum: 000 0111 1000 (bin) 120 (dec) (120° C) Maximum: 000 1010 0101 (bin) 165 (dec) (165° C) Note: Any values written to read-only registers are ignored.

Table. OT_FAULT THRESHOLD Settings

TEMPERATURE (°C)(1)	OT_FAULT_THRESHOLD (°C BIN)	**TEMPERATURE (°C)**	**OT_FAULT RESET THRESHOLD (°C BIN)**
120	01111000	100	01100100

125	01111101	105	01101001
130	10000010	110	01101110
135	10000111	115	01110011
140	10001100	120	01111000
145	10010001	125	01111101
150	10010110	130	10000010
155	10011011	135	10000111
160	10100000	140	10001100
165	10100101	145	10010001

(1) Lists only multiples of 5° C; but, the actual LSB is 1°C.

OT_WARN_LIMIT (5Ih)

Format	Literal (5-bit two's SHARE3 lement exponent, 11-bit two's SHARE3 lement mantissa)
Description	The OT_WARN_LIMIT command sets the value of the temperature, in degrees Celcius, which causes an over-temperature warning condition. • Sets the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Sets the OTW bit in the STATUS_TEMPERATURE register • Notifies the host (Asserts SMB_ALERT) OT_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_WARN_LIMIT should always be set to less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than OT_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 01111000 (binary) The default setting results in a real OT_WARN_LIMIT of 120° C. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (1° C) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the Mantissa for the linear format. Default: 000 01111000 (bin) 120 (dec) (120° C) Minimum: 000 0110 0100 (bin) 100 (dec) (100° C) Maximum: 000 1000 1100 (bin) 140 (dec) (140° C) Note: Any values written to read-only registers are ignored.

Table. OT_WARN_LIMIT Settings

TEMPERATURE (°C)(1)	OT_FAULT_THRESHOLD (°C BIN)	**TEMPERATURE (°C)**	**OT_FAULT RESET THRESHOLD (°C BIN)**
100	01100100	80	1010000
105	01101001	85	1010101

110	01101110	90	1011010
115	01110011	95	1011111
120	01111000	100	1100100
125	01111101	105	1101001
130	10000010	110	1101110
135	10000111	115	1110011
140	10001100	120	1111000

(1) Lists only multiples of 5° C; but, the actual LSB is 1°C.

TON_RISE (61h)

Format	Linear
Description	The TON_RISE command sets the time in ms, from when the reference VREF starts to rise until it reaches the end value. It also determines the rate of transition of the reference VREF (either due to VREF_TRIM or STEP_VREF_MARGIN_HIGH/ STEP_VREF_MARGIN_LOW commands), when this transition is executed during the soft-start state. Values written within the supported range of TON_RISE are mapped to the nearest supported increment. TON_RISE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default setting results in TON_RISE of 2.7ms The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 μs) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) This is the Mantissa for the linear format. Default: 000 0010 1011 (bin) 43 (dec) (equivalent to 2.688 ms) Minimum: Any value equal or less than 12 dec is equivalent to the min 600 μs Maximum: Any value greater than 120 dec is equivalent to 9 ms Note: Any values written to read-only registers are ignored.

Table . Allowable TON_RISE Values

TON_RISE TIME (ms)	MANTISSA (BINARY)
0.6	000 0000 1010
0.9	000 0000 1110
1.2	000 0001 0011
1.8	000 0001 1101
2.7	000 0010 1011
4.2	000 0100 0011
6	000 0110 0000
9	000 1001 0000

STATUS_BYTE (78h)

Format	Unsigned binary
Description	The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. STATUS_BYTE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults – OVF, UVF, PGOOD are only be set for that slave's master (which may be in the other IC for 3-ph and 4-ph systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_BYTE register also reports communication faults in the Other Faults bit.
Default	0x000000 (binary)

7	6	5	4	3	2	1	0
0	OFF	OVF	OCF	VIN_UV	OTFW	cml	oth

Bits	Field Name	Description
7	0	Default: 0
6	OFF	(Format: binary) Output is OFF This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Unit is on 1: Unit is off
5	OVF	(= VOUT_OV in PMBus Specification) (Format: binary) Output Over-Voltage Fault Triggers SMB_ALERT. For a slave configuration, this bit is set to 0. 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
4	OCF	(=IOUT_OC in PMBus Specification) (Format: binary) Output Over-Current Fault 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
3	VIN_UV	(Format: binary) Input voltage (VIN) under-voltage fault. This bit is defined only on PAGE0. For PAGE1, this bit is 0. This bit is masked before soft-start is finished. 0: (Default) An input under-voltage fault has not occurred. 1: An input under-voltage fault has occurred.
2	OTFW	(= TEMPERATURE in PMBus Specification) (Format: binary) Over-Temperature Fault/warning OTF or OTW input has been asserted by the external sensor for that channel. 0: (Default) An over-temperature fault or warning has not occurred. 1: An over-temperature fault or warning has occurred.
1	cml	(= CML in PMBus Specification) (Format: binary) Communications, memory or logic fault has occurred. This bit is used to flag communications, memory or logic faults. 0: (Default) A communications, memory or logic fault has not occurred 1: A communications, memory or logic fault has occurred

0	oth	(= NONE OF THE ABOVE in the PMBus Specification) (Format: binary) Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (7:1) in this register. 0: (Default) A fault or warning not listed in bits (7:1) has not occurred. 1: A fault or warning not listed in bits (7:1) has occurred.

STATUS_WORD (79h)

Format	Unsigned binary
Description	The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. STATUS_WORD is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. If PAGE command is set to 11, then PAGE 0 of the status register is read. The STATUS_WORD also reports a power good fault. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults (OVF, UVF, PGOOD) are be set only for that slave's master (which may be in the other device for 3-phase and 4-phase systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_WORD also reports communication faults in the Other Faults bit.
Default	000000000x000000 (binary)

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1
VF	OCFW	0	MFR	PGOOD_Z	0	0	0	0	OFF	OVF	OCF	VIN_UV	OTFW	cml

Bits	Field Name	Description
7	VF	(= VOUT in the PMBus Specification) (Format: binary) Voltage Fault = (OVF + UVF) For slave configurations, this bit is set to 0. 0: (Default) An output voltage fault or warning has not occurred. 1: An output voltage fault or warning has occurred.
6	OCFW	(= IOUT/POUT in the PMBus Specification) (Format: binary) Output Current Fault OR Warning = (OCF + OCW) 0: (Default) An output over-current fault or warning has not occurred. 1: An output over-current fault or warning has occurred.
5	0	Default: 0
4	MFR	(= MFR in the PMBus Specification) (Format: binary) Internal thermal fault (from bandgap) Thermal shutdown fault for the IC 0: (Default) An internal TSD has not occurred. 1: An internal TSD has occurred.
3	PGOOD_Z	(= POWER_GOOD# in the PMBus Specification) (Format: binary) Power Good Fault (in effect, Power Good Indication - Inverted) The Power Good fault is used to flag when the converter output voltage rises or falls outside of the PGOOD window. If the channel is configured as a slave, this bit are set to "0" (PGOOD_Z is only reflected in the master). 0: (Default) A Power Good fault is not present. 1: Device-channel experiencing a Power Good fault.
2:0	0	Default: 0

The STATUS_WORD low byte is the STATUS_BYTE.

STATUS_VOUT (7Ah)

Format	Unsigned binary
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The PMBus core is notified of these fault conditions via the 2 input pins labeled OVF and UVF. The PMBus core then communicates these faults to the host through its serial communication channel. STATUS_VOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OVF	0	0	UVF	0	0	0	0

Bits	Field Name	Description
7	OVF	(= VOUT OV Fault in the PMBus Specification) (Format: binary) Output Over-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
6:5	0	Default: 0
4	UVF	(= VOUT UV Fault in the PMBus Specification) (Format: binary) Output Under-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). The UV fault indicates only an under-voltage condition at the Trim pin and may not necessarily reflect an over-current situation. However, during an output crowbar short condition, the Trim may sag below the UV threshold level before the current reaches the OC threshold, resulting in a UV fault. If the IOUT_OC_FAULT_RESPONSE register is selected to the retry setting, and the output short is persistent, an over-current fault are triggered for subsequent start-up retry attempts. 0: (Default) An output under-voltage fault has not occurred. 1: An output under-voltage fault has occurred.
3:0	0	Default: 0

STATUS_IOUT (7Bh)

Format	Unsigned binary
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The PMBus core is notified of these fault conditions via the inputs OCF and OCW. STATUS_IOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OCF	0	OCW	0	0	0	0	0

Bits	Field Name	Description
7	OCF	(= IOUT OC Fault in the PMBus Specification) (Format: binary) Output Over-Current Fault Set based upon the value stored in IOUT_OC_FAULT_LIMIT 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
6	0	Default: 0
5	OCW	(= IOUT OC Warning in the PMBus Specification) (Format: binary) Output Over-Current Warning Set based upon the value stored in IOUT_OC_WARN_LIMIT. 0: (Default) An output over-current warning has not occurred. 1: An output over-current warning has occurred.
4:0	0	Default: 0

STATUS_TEMPERATURE (7Dh)

Format	Unsigned binary
Description	The STATUS_ TEMPERATURE command returns one byte of information relating to the status of the converter's die temperature related faults. STATUS_TEMPERATURE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OTF	OTW	0	0	0	0	0	0

Bits	Field Name	Description
7	OTF	(= OT Fault in the PMBus Specification) (Format: binary) Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	(= OT Warning in the PMBus Specification) (Format: binary) Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5:0	0	Default: 0

STATUS_CML (7Eh)

Format	Unsigned binary
Description	The STATUS_ CML command returns one byte containing PMBus serial communication faults.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
ivc	ivd	pec	mem	0	0	oth	0

Bits	Field Name	Description
7	ivc	(= Invalid/Unsupported Command in the PMBus Specification) (Format: binary) Invalid or unsupported Command Received 0: (Default) Invalid or unsupported Command not Received. 1: Invalid or unsupported Command Received. An attempt to write an invalid PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
6	ivd	(= Invalid/Unsupported Data in the PMBus Specification) (Format: binary) Invalid or unsupported data Received 0: (Default) Invalid or unsupported data not Received. 1: Invalid or unsupported data Received.
5	pec	(= Packet Error Check Failed in the PMBus Specification) (Format: binary) Packet Error Check Failed This is a CRC byte sent at the end of each data packet. It is implemented as CRC(x) = x8 + x2 + x1 + 1 0: (Default) Packet Error Check Passed 1: Packet Error Check Failed
4	mem	(= Memory Fault Detected in the PMBus Specification) (Format: binary) Memory Fault Detected This bit indicates a fault with the internal memory. 0: (Default) No fault detected 1: Fault detected
3:2	0	Default: 0
1	oth	(= Other Communication Fault in the PMBus Specification) (Format: binary) Other Communication Fault 0: (Default) A communication fault other than the ones listed in this table has not occurred. 1: A communication fault other than the ones listed in this table has occurred.
0	0	Default: 0

STATUS_MFR_SPECIFIC (80h)

Format	Unsigned binary
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
otfi	x	x	ivaddr	ch1_sps_SHARE 1	ch2_sps_SHARE 1	ch1_slave	ch2_slave

Bits	Field Name	Description
7	otfi	(Format: binary) over-temperature fault internal. This bit is required to distinguish an over-temperature fault internal to the device from an external temperature fault. 0: (Default) The internal temperature is below the fault threshold. 1: The internal temperature is above the fault threshold.
6:5	x	Default: 0

4	ivaddr	(Format: binary) Invalid PMBus address This bit is set when the PMBus address detection circuit does not resolve to a valid address. In this event, the device responds to the address: 127d. 0: (Default)
3	ch1_sps_SHARE1	(Format: binary) Channel 1 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
2	ch2_sps_SHARE1	(Format: binary) Channel 2 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
1	ch1_slave	(Format: binary) Channel 1 Slave This bit is set when channel 1 is configured as a slave channel (by pulling FB1 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)
0	ch2_slave	(Format: binary) Channel 2 Slave This bit is set when channel 2 is configured as a slave channel (by pulling FB2 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)

READ_VOUT (8Bh)

Format	Linear
Description	The READ_VOUT command returns two bytes of data in the linear data format that represent the output voltage. The exponent is set to －9 by VOUT_MODE. VOUT = Mantissa x $2^{Exponent}$ READ_VOUT is a paged register. In order to access READ_VOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_VOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE register cannot be set to 11 for READ_VOUT command.
Default	0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															

Bits	Field Name	Description
7：0	Mantissa	(Format: unsigned binary) This is the Mantissa for the linear format. Default: 0000 0000 0000 0000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_IOUT (8Ch)

Format	Linear
Description	The READ_IOUT command returns the output current in amps for each channel. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). Note: only positive currents are reported. Any SHARE3uted negative current (For example, 0 measured current and －4 A IOUT_CAL_OFFSET) is reported as 0 A. READ_IOUT is a paged register. In order to access READ_IOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_IOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE(7),(0) register cannot be set to 11 for READ_IOUT command.
Default	E0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7：3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 mA lsb) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) Default: 000 00000000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_TEMPERATURE_2 (8Eh)

Format	Linear
Description	The READ_TEMPERATURE_2 command returns the temperature in degrees Celsius of the current channel specified by the PAGE command.
Default	F064h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11110 (bin) －2 (dec) 0.25° C These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) Default: 000 0110 0100 (bin) 100 (dec) Note: Any values written to read-only registers are ignored.

PMBus_REVISION (98h)

Format	Linear
Description	The PMBus_REVISION command returns the revision of the PMBus to which the device is SHARE3liant. The device is SHARE3liant to revision 1.1 of the PMBus specification.
Default	00010001b

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	/	/

MFR_SPECIFIC_00 (D0h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_00 register is dedicated as a user scratch pad
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0		

MFR_SPECIFIC_04 (VREF_TRIM) (D4h)

Format	Linear
Description	The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_x) × 2 mV The maximum trim range is 10% / - 20% of nominal VREF (600 mV) in 2-mV steps. Permissible values are from 60 mV to - 120 mV. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to - 180 mV. If the commanded VREF_TRIM is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. The VREF_TRIM has two data bytes formatted as two' s SHARE3 lement binary integer and can have positive and negative values. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command is ignored. (In analog, the master programmed value are used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command, or when in AVS mode results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000h (Fixed Offset Voltage = 0 V) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) (sign extended) Bits 6:0 changes for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: binary) Default: 0000 0000 (bin) 0 (dec) 0 mV Minimum: 1100 0100 (bin) –60 (dec) (–120 mV) (sign extended, twos SHARE3liment) Maximum: 0001 1110 (bin) 30 (dec) (60 mV) Bits 7:6 changes for sign extension but are not otherwise programmable

MFR_SPECIFIC_05 (STEP_VREF_MARGIN_HIGH) (D5h)

Format	Linear
Description	The STEP_VREF_MARGIN_HIGH command is used to increase the value of the reference voltage by shifting the reference higher. When the OPERATION command is set to Margin High, the reference increases by the voltage (in mV) indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_HIGH) × 2 mV

	The maximum range is 0 to 10% (60 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to －180 mV. If the commanded STEP_VREF_MARGIN_HIGH is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital). An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000 0000 0001 1110 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 0000 0000 (bin) Maximum: 0000 0000 (bin) Note: Any values written to read-only registers are ignored.
7:0	Low Byte	(Format: binary) This specifies a positive offset voltage on to default VREF. Default: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent) Minimum: 0000 0000 (bin) 0 (dec) (0 mV) Maximum: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent)

MFR_SPECIFIC_06 (STEP_VREF_MARGIN_LOW) (D6h)

Format	Linear
Description	The STEP_VREF_MARGIN_LOW command is used to decrease the reference voltage by shifting the reference lower. When the OPERATION command is set to Margin Low, the output decreases by the voltage indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VOUT_MARGIN_LOW) × 2 mV .The maximum range is 0 to－20% (－120 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to－180 mV. If the commanded STEP_VREF_MARGIN_LOW is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF is set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1111 1110 0010 (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 1111 1111 (bin) (msb is sign bit) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) Bits 6:0 can change for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: two's SHARE3 lement) This specifies a negative offset voltage on to default VREF. Default: 1110 0010 (bin) -30 (dec) (–60 mV = –10% percent) Minimum: 1100 0100 (bin) -60 (dec) (–120 mV = –20% percent) Maximum: 0000 0000 (bin) 0 (dec) (0 mV) Bits 7:6 can change for sign extension but are not otherwise programmable

MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h)

Format	Unsigned binary integer
Description	The PCT_VOUT_FAULT_PG_LIMIT is to set the PGOOD, VOUT_UV and VOUT_OV limits. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	XXXX XX10 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PG(1:0)

Bits	Field Name	Description
7:2	X	X indicates writes are ignored and reads are 0
1:0	PG(1:0)	(Format: binary) PG, UV, OV Limit Selection. Default: 10

Table lists the over-voltage, under-voltage, and power-good threshold voltages. Bit (13) of MFR_SPECIFIC_16 (E0h) register determines the over-voltage setting.

Table. OV, UV, PGOOD Threshold Values

PG(1)	PG(0)	UV_fault (%)	PG_low (%)	PG_high (%)	OV_fault		OV SETTING
					(%)	(mV)	
0	0	- 16.8	- 12.5	12.5	16.8	n/a	Tracking
0	1	- 12.0	- 7.0	7.0	12.0		
1	0	-29.0	- 23.0	7.0	16.8		
1	1	- 29.0	- 23.0	7.0	12.0		
0	0	- 16.8	- 12.5	12.5	N/A	800	Fixed
0	1	- 12.0	- 7.0	7.0		700	
1	0	- 29.0	- 23.0	7.0		800	
1	1	- 29.0	- 23.0	7.0		700	

MFR_SPECIFIC_08 (SEQUENCE_TON_TOFF_DELAY) (D8h)

Format	Unsigned binary integer
Description	The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and the delay for turning off the device as a ratio of TON_RISE. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. In such a case, internally the TON_DELAY is set to the minimum value of 50 μs and TOFF_DELAY is set to zero (overriding any contents of EEPROM). An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	111X 000X (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
TON_DEL<2:0>			X	TOFF_DEL<2:0>			X

Bits	Field Name	Description
7:5	TON_DEL<2:0>	(Format: binary) Default: 111b TON_DELAY = TON_RISE × TON_DEL<2:0> This parameter controls the delay from when ON = 1 until soft-start sequence begins. The default value is 18.9 ms. (Start the VOUT ramp without delay)
4	X	X indicates writes are ignored and reads are 0
3:1	TOFF_DEL<2:0>	(Format: binary) Default: 000b TOFF_DELAY = TON_RISE x TOFF_DEL<2:0> This parameter controls the delay from when ON = 0 until the output is disabled. The default value is 0 ms. (Shut off the output without delay)
0	X	X indicates writes are ignored and reads are 0

Table . Delay Time Ratios

TON_DEL<2:0> TOFF_DEL<2:0>	DELAY TIME RATIO (MULTIPLE OF TON_RISE)
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

NOTE:

If the device turns off due to a turn-off delay time, any attempt to turn on the device before the turn-off delay time expires should be avoided. The device is available to be turned on only after the turn-off delay time expires and the device has been turned off.

MFR_SPECIFIC_16 (COMM_EEPROM_SPARE)(E0h)

Format	Unsigned binary
Description	This register contains EEPROM backed bits brought out to the top of the digital block IO for possible future use by analog or digital circuits
Default	1011 0001 xxxx x011 (binary) The default power-up state can be changed using the STORE_USER commands.

COMM_EEPROM_SPARE							
r/w^E	r/w^E	r/w^E	r/w^E	r	r	r	r
15	14	13	12	11	10	9	8
PGOOD_DEL_EN	DIS_API_CNT	FIX_OVP_EN	DIS_SSPB				

COMM_EEPROM_SPARE							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0

Bits	Field Name	Description
15	PGOOD_DLY_EN	(format: binary, access: read/write) Default: 1b PGOOD Delay Enable This bit, when high, enable 2-ms delay for PGOOD detection during startup.
14	DIS_API_CNT	(format: binary, access: read/write) Default: 0b Disables 3-clock count for API valley active state This bit, when high, disables the 3-clock counter for API valley. When the bit is low, the counting is enabled whereby the API-valley function can remain active only 3 consecutive clock cycles before being inactive for another 3 clocks.
13	FIX_OVP_EN	(Format: binary, access: read/write) Default: 1b Enable fixed output voltage OV protection This bit, when high, enables fixed OV protection circuitry that is active after the BP3 and BP5 voltage comes up. When the bit is low, tracking OV protection is enabled instead and in this case, OV protection is enabled only after the soft-start sequence has SHARE3leted.
12	DIS_SSPB	(Format: binary, access: read/write) Default: 1b Disable pre-bias initiation after soft-start sequence has SHARE3leted. This bit affects the PWM signal only during prebias startup. When this bit is high, PWM switching begins only if the SHARE3 voltage is higher than the PWM ramp valley. When this bit is low, PWM switching is forced to begin after soft-start sequence has SHARE3leted, even when the SHARE3 voltage is lower than PWM ramp valley.

MFR_SPECIFIC_21 (OPTIONS) (E5h)

Format	Unsigned binary
Description	This register is used for setting user selectable options for the controller.
Default	0111 1111 0000 0000 (binary) The default power-up state can be changed using the STORE_USER commands.

Common/Shared							
r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w
7	6	5	4	3	2	1	0
TCO	CH2_CSGAIN_SEL<2:0>		CH1_CSGAIN_SEL<1:0>		en_adc_cntl	EN_TSNS_SHARE1	EN_SPS
r	r	r	r	r	r	r/w^E	r/w
						SMB_OV	msps_SHARE1

Bits	Field Name	Description
7	TCO	(Format: binary) Default: 0b Temperature SHARE3ensation override 0: OCF, OCW thresholds and current measurements are temp SHARE3ensated 1: Temperature SHARE3ensation is "disabled" TCO is a non-paged bit. Any change on TCO bit is applied to both page 0 and page 1.
6:5	CH2_CSGAIN_SEL<1:0>	(Format: binary) 1:0> Default: 11b Ch2 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 2. For high DCR/L ratios, the user can select lower gains for current-loop stability.
4:3	CH1_CSGAIN_SEL<1:0>	(Format: binary) Default: 11b Ch1 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 1. For high DCR/L ratios, the user can select lower gains for current-loop stability. 00: 50 V/V gain 01: 40 V/V gain 10: 30 V/V gain 11: 20 V/V gain
2	en_adc_ctl	(Format: binary) Default: 1b Enable ADC Control Bit. 0: Disable ADC operation. 1: Enable ADC operation.
1	EN_TSNS_SHARE1	(Format: binary) Default: 1b Enable fault input from Smart power stage This bit, when high, makes the device sensitive to fault communication from the smart power stage. When this bit is low, the device ignores the fault indication from the smart power stage. Whether this bit is high or low, the device performs over-temperature protection and declares OT fault when Smart power stage temperature is above the OT fault threshold.
0	EN_SPS	(Format: binary) Default: 1b(forbid change)
7:2		Note: Any values written to read-only registers are ignored.
1	SMB_OV	(Format: binary) Default: 0b Make SMBALERT an OV fault indicator. This has page 0 scope only (in effect, it is defined only on page 0; the page 1 bit is not used). 0: SMBALERT functions normally 1: SMBALERT reports only OV_FAULT
0	msps_SHARE1	(Format: binary) Default: 0b (PAGE scope) 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(3) / STATUS_MFR_SPECIFIC(2) (corresponding to the CH1_SPS_SHARE1 and CH2_SPS_SHARE1 respectively).

MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h)

Format	Unsigned binary
Description	This register is used for setting user selectable PWM phase configuration (sync enable, direction of frequency synchronization pulses - in or out - in a master channel and number of phases) in a multi-phase system.
Default	0001h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
											SYNC_MODE<1:0>		ENSYNC	PHASE	

Bits	Field Name	Description
7:0 7:5		Note: Any values written to read-only registers are ignored.
4:3	SYNC_MODE<1:0>	(Format: binary) Default: 00b Synchronization configuration for the oscillator These bits allow the user to configure the internal PWM oscillator clock in the PWM master channel 1 in one of several operating modes as described below. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then these bits are internally forced to <1:1> indicating that external signals on the SYNC and PHDET pins must override the internal clock and phase zero signals. In a case of slave channel 1, any attempt to write a "0" to either one or both bits are treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Self generated clock with internal phasing, switch positions 1 and 3 01: External clock on SYNC pin, but phasing is internal; switch positions 1 and 3 10: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 1 and 3 11: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 2 and 4 (forced for channel 1 slave)
2	ENSYNC	(Format: binary) Default: 0b Synchronization enable This bit, when high, enables the synchronization drivers. 0: Synchronization is disabled 1: Synchronization is enabled
1:0	PHASE	(Format: binary) Default: 01b Number of phases in the system (that involves the IC). This pair of bits is used to configure the number of phases in the power-supply system containing the IC. This information is then used inside the PWM oscillator to set the master switching frequency and channel phase angles. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then the bit PHASE <1> is internally forced to 1 indicating that only 3-ph or 4-ph modes can be enabled. In such a case of slave channel 1, any attempt to write a "0" to this bit is treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Independent, dual channel operation 01: Two-phase operation (within single IC) 10: Three-phase operation (between two ICs) 11: Four-phase operation (between two ICs)

NOTE:

A 120° phase shift can be achieved between three phases at 3-phase plus 1-phase configuration, the 1-phase rail has the same phase as channel 1 of the master IC.

A 90° phase shift can be achieved between all four phases at all other configurations listed in the table. SYNC pins of two devices need to be connected, and SHARE2 pins of two devices need to be connected.

Table. Phase Configurations(1)

PHASE CONFIGURATIONS	MASTER IC			SLAVE IC		
	SYNC_MODE	ENSYNC	PHASE	SYNC_MODE	ENSYNC	PHASE
3-phase + 1-phase	00	1	10	11	1	10
4-phase	00	1	11	11	1	11
2-phase + 2-phase	00	(2)	11	11	(2)	11
2-phase + dual-output	00	(2)	11	11	(2)	11
Dual-output + dual-output	00	(2)	11	11	(2)	11

(1) For 3-phase plus 1-phase configuration and 4-phase configuration, SYNC_MODE, ENSYNC and PHASE can be programmed, saved to EEPROM at one time and then reboot the device for the new value to take effect.

(2) For all other configurations listed in the table, follow these steps to program two devices to avoid potential damage.

1. Set ENSYNC to 0 on each device.
2. Program SYNC_MODE and PHASE correctly at both devices, save to the EEPROM and then reboot the devices.
3. Set ENSYNC to 1 on each device to enable synchronization between two devices. No reboot is needed.

MFR_SPECIFIC_23 (MASK SMBALERT) (E7h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_23 (MASK SMBALERT) command may be used to prevent a warning or fault condition from asserting the SMBALERT signal. This command is unique in that it is partially paged; and partially common/shared – since some faults are channel dependent; and others are channel independent. The upper 8 bits of this register always controls and accesses the shared/common set of faults, regardless of the (00h) PAGE setting. However, the control and access for the lower 8 bits of this register are (00h) PAGE dependent and controls or reflects the currently selected page. Only provides below two options for MASK_SMBALERT setting. ● When en_auto_ARA bit (auto Alert Response Address response) is enabled, all other bits in this PMBus register need to be disabled. ● When en_auto_ARA bit is disabled, any other bits in this PMBus register can be set as desired.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

Common/Shared								PAGE0, PAGE1							
r/w	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w^E	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
motfi	mprtcl_err	msmb_TO_err	mivc	mivd	mpec	mmem	en_auto_ARA	mOTF	mOTW	mOCF	mOCW	mOVF	mUVF	mPGOOD_Z	mVIN_UV

Bits	Field Name	Description
7	motfi	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(7)

6	mprtcl_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB Protocol Error from the PMBus interface module. One of 2 sources is STATUS_CML(1).
5	msmb_TO_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB_TIMEOUT from the PMBus interface module. One of 2 sources is STATUS_CML(1).
4	mivc	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(7)
3	mivd	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(6)
2	mpec	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(5)
1	mmem	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(4)
0	en_auto_ARA	(Format: binary) Default: 0b Enables auto Alert Response Address response. When this feature is enabled, the hardware automatically masks any fault source currently set from re-asserting SMB_ALERT when this device responds to an ARA on the PMBus. This prevents PMBus "bus hogging" in the case of a persistent fault in a device that consistently wins ARA arbitration due to its device address. In contrast, when this bit is cleared, immediate re-assertion of SMB_ALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually. When WRITE_PROTECT is set to 20h, 40h or 80h, en_auto_ARA is enabled automatically.
7	mOTF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(7)
6	mOTW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(6)

5	mOCF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(7)
4	mOCW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(5)
3	mOVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(7)
2	mUVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(4)
1	mPGOOD_Z	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_WORD(11)
0	mVIN_UV	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_BYTE(3)

MFR_SPECIFIC_30 (TEMP_OFFSET) (EFh)

Format	Unsigned binary
Description	This paged register is used for setting user selectable offset in the measured temperature. The specified offset value is added to the post-math digital output. The new, post-offset, post-averaging temperature is used for READ_TEMP_2 reporting and for temperature SHARE3ensation of IOUT_CAL_GAIN for both reporting READ_IOUT, and OC_FAULT_LIMIT/WARN threshold setting.
Default	F800h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r	r	r	r	r	r	r	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3 lement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (LSB = 0.5 deg) These default settings are not programmable.
2:0 7:0	Mantissa	(Format: two's SHARE3 lement) Default: 000 (bin) 0 (dec) (0 deg) Minimum 7F8 = –8 x 0.5 deg = –4 deg Maximum 006 = 6 x 0.5 deg = 3 deg

MFR_SPECIFIC_32 (API_OPTIONS) (F0h)

Format	Unsigned binary
Description	This paged, user-accessible register is used for setting the API SHARE3arator thresholds and other related options.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
										API_VAL_HIGH	API_VAL_EN	API_AVG	API_EN	API_SET<1:0>	

Bits	Field Name	Description
7:0 7:6		Note: Any values written to read-only registers are ignored.
5	API_VAL_HIGH	(Format: binary) Default: 0b API valley high threshold When this bit is high, the detection threshold for the API valley circuit is increased to approximately 100 mV from the default value of 50 mV.
4	API_VAL_EN	(Format: binary) Default: 0b API valley enable When this bit is high, API valley circuit is enabled to improve load-dump transient response. When the SHARE3 voltage drops suddenly during load-dump and the variation of SHARE3 voltage exceeds the threshold, the API valley function is triggered. As a result, both high-side and low-side switches are turned off to force the load current go through the body diode of low-side switch to reduce output voltage spike.
3	API_AVG	(Format: binary) Default: 0b API average mode When this bit is high, API circuit uses average value of SHARE3 instead of peak value for threshold detection.
2	API_EN	(Format: binary) Default: 0b API enable When this bit is high, API circuit is enabled to improve load step-up transient response. When the SHARE3 voltage goes high suddenly during load step-up and the variation of SHARE3 voltage exceeds the threshold, the API function is triggered. As a result, additional pulses are injected to reduce output voltage dip 0: API is disabled 1: API is enabled
1:0	API_SET<1:0>	(Format: binary) Default: 00b API SHARE3arator threshold setting This is a 2-bit user setting for selecting the appropriate API SHARE3arator threshold. 00: 35 mV 01: 60 mV 10: 85 mV 11: 110 mV

MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format	Unsigned binary
Description	The DEVICE_CODE command returns a 12-bit unique identifier code for the device and a 4-bit device revision code.
Default	01E0h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0 7:4	Identifier Code	0000 0001 1110b : Device ID Code Identifier for the device
3:0	Revision Code	0000b : Revision Code (first silicon starts at 0)

Note:

1. For additional information on Product Packaging please refer to www.mornsun-power.com. Packaging bag number: 58210317;
2. If the product is not operated within the required load range, the product performance cannot be guaranteed to comply with all parameters in the datasheet;
3. The maximum capacitive load offered were tested at input voltage range and full load;
4. Unless otherwise specified, parameters in this datasheet were measured under the conditions of Ta=25℃, humidity<75%RH with nominal input voltage and rated output load;
5. All index testing methods in this datasheet are based on our company corporate standards;
6. We can provide product customization service, please contact our technicians directly for specific information;
7. Products are related to laws and regulations: see "Features" ;
8. Our products shall be classified according to ISO14001 and related environmental laws and regulations, and shall be handled by qualified units.

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